APPLICATION NOTE

ABSTRACT
The SA8027 is a low voltage, low phase noise, fractional-N frequency synthesizer. It is targeted for wireless systems where good phase noise performance and fast switching time is crucial. The SA8027 is pin-for-pin compatible with the SA8026 but delivers the same AC performance at reduced DC current consumption.

AN10159

SA8027: 2.5 GHz fractional-N 550 MHz IF integer frequency synthesizer

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2002 Jun 26

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AN10159

1.0 Introduction to the SA8027

The SA8027 is fabricated in QUBiC 3 Silicon BiCMOS process and integrates three programmable dividers, three charge pumps and two phase comparators to implement a main fractional–N phase locked loop that is capable of operating up to 2.5 GHz. In addition, a second auxiliary phase locked loop is incorporated that is capable of operating up to 550 MHz. The device is designed to function down to 2.7 volts, which is compatible with three NiCad cell operation.

The SA8027 is programmed by a three-wire serial bus capable of clock rates up to 10 MHz. The main, auxiliary and reference dividers are programmed via the 3–wire bus. The SA8027 is designed with three user registers of twenty–four bits each.

The part has three ground pins, one digital and two analog, which should be externally connected together. Large current could flow across the die if the connection is not implemented resulting in possible failure of the part.

By design, voltage applied to the V_{DD} and V_{DDCP} pins are limited to 3.6 volts. The voltage at the V_{DDCP} pin can be equal to or greater than that at the V_{DD} pin, but not greater than the specified 3.6 volt upper limit.

Signal power to the RFin and AUXin pins should be between the specified levels as indicated in the SA8027 data sheet or unpredictable operation may occur. The data sheet can be found on the Web at the following URL: http://www.semiconductors.philips.com.

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2.0 Overview

2.1 Block diagram

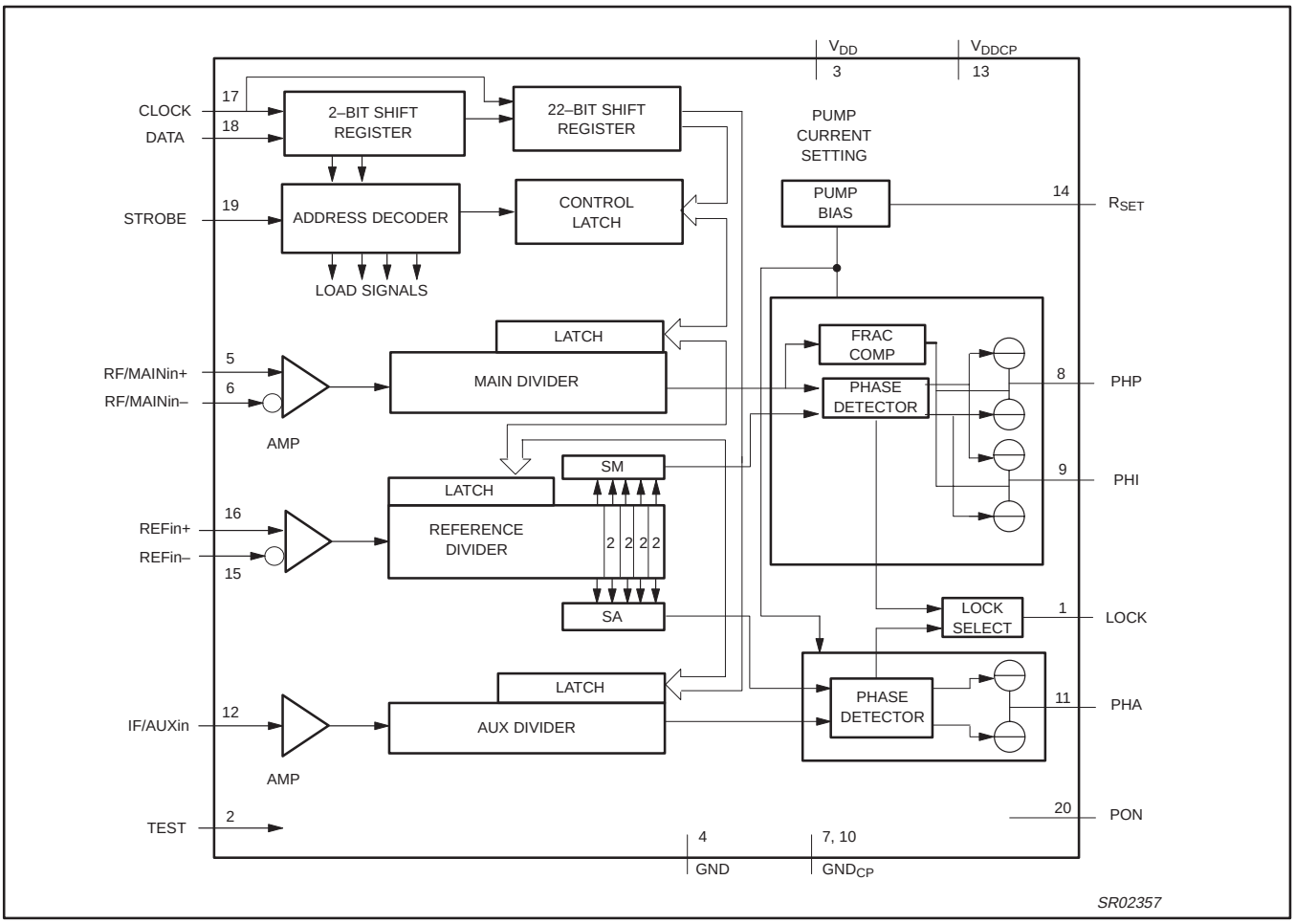


Figure 1. Block diagram of the SA8027 in the TSSOP package.

2.2 Features

- Main synthesizer operating frequency up to 2.5 GHz
- Modulus select of 5 or 8
- Main synthesizer fractional spur compensation
- Auxiliary synthesizer frequency range up to 550 MHz
- User controllable speed up mode
- Programmable charge pump current levels
- Low phase noise
- Low power consumption

3.0 Functional description

3.1 Fractional compensation

Figure 2 is a block diagram of the fractional compensation method implemented in the SA8027.

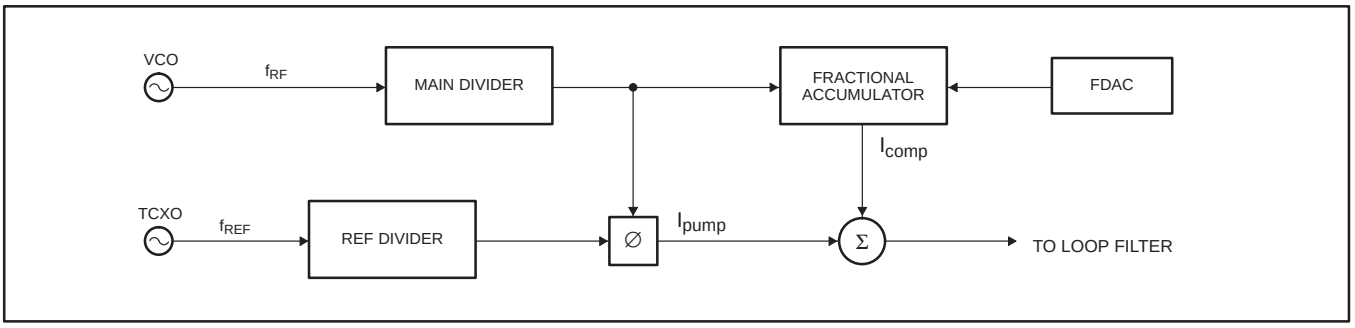


Figure 2. Fractional compensation method: current injection.

The fractional compensation current is added to the charge pump output currents, I_{php} and I_{phi}, via an 8-bit fractional compensation DAC (FDAC) to reduce the fractional spurs. I_{php} is the main charge pump and I_{phi} is a secondary charge pump used to supply an additional amount of speed-up current to the main loop filter if needed. Design target is for 15 dB of compensation over all operating conditions with theoretical FDAC values of 80 for FMOD = 8 or 128 for FMOD = 5. **The optimum FDAC value however, will be dependent upon board layout as well as supply voltage.** Best fractional spur rejection is achieved by optimizing the FDAC value for each device.

The compensation current generated is:

$$I_{comp} = \frac{I_{pump}}{128} \times \frac{FDAC}{5 \times 128} \times FRD$$

If FDAC is fixed, the compensation current is then directly proportional to the value contained in the fractional accumulator (FRD).

3.1.1 FDAC derivation

At every cycle, the VCO advances on the reference by FRD/FMOD of the VCO cycle. The instantaneous phase error is then:

$$\frac{FRD}{FMOD} \times \frac{1}{VCO}$$

Where FMOD is the modulus used. Therefore, the extra charge taken from the filter is:

$$Q_n = \frac{FRD \times I_{pump}}{FMOD \times VCO}$$

To compensate for this charge, an equal amount of charge is added to the filter.

$$Q_{comp} = \frac{I_{pump}}{128} \times \frac{FDAC}{5 \times 128} \times \frac{128FRD}{VCO} + \frac{I_{pump} \times FDAC \times FRD}{640 \times VCO}$$

Setting $Q_n = Q_{comp}$ and solving for FDAC

$$\frac{FRD \times I_{pump}}{FMOD \times VCO} = \frac{I_{pump} \times FDAC \times FRD}{640 \times VCO} = FDAC = \frac{640}{FMOD}$$

3.2 Analog fractional compensation

Figures 3 and 4 show the uncompensated and compensated fractional spur response. 20 dB suppression with respect to FDAC = 0 is typically achievable over temperature, voltage, and frequency assuming no adjustment of FDAC. The two figures were recorded with f_{comp} = 1000 kHz, NF = 1, and FMOD = 5. In Figure 3 FDAC = 0, while in Figure 4 FDAC was adjusted for optimal fractional spur rejection, i.e. FDAC = 118.

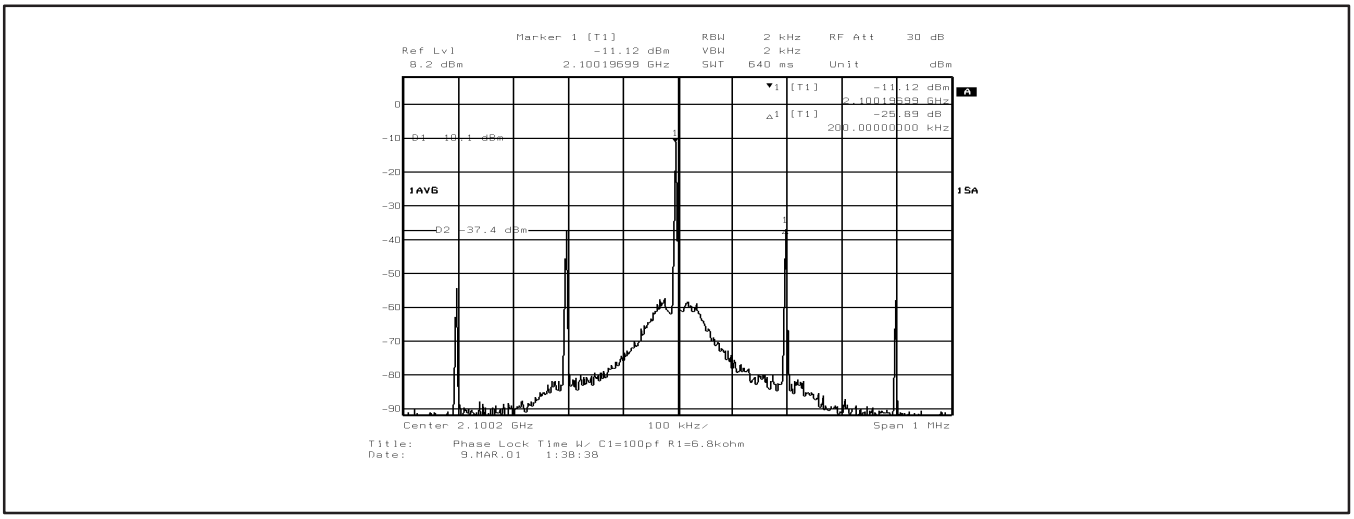


Figure 3. Uncompensated 200 kHz spur at –26 dBc typ.

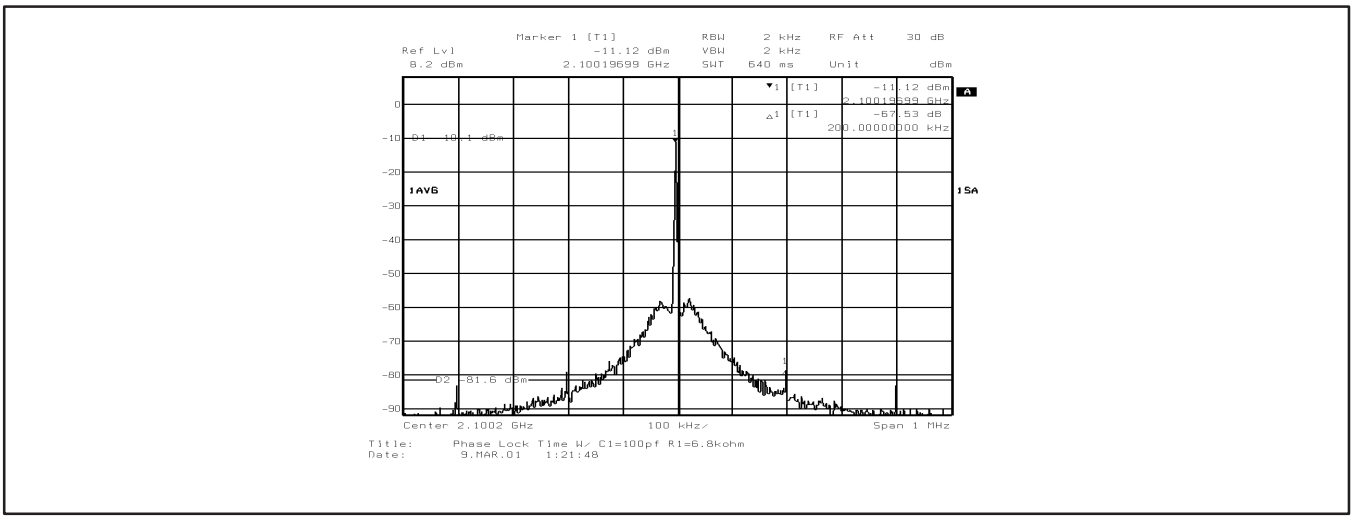


Figure 4. Compensated 200 kHz spur at –67 dBc typ.

Note that the theoretical or expected optimal FDAC value is 128 for FMOD = 5. Near the optimal value, small variations in FDAC value can result in a degradation of fractional suppression which can vary as much as 6 dB for ±2 counts of FDAC. The shape of this curve will be the same from device to device, but may be shifted by ±2 FDAC counts. The plot in Figure 5 was generated with the modulus set to 5 and shows the variation in fractional suppression with FDAC. The plot shows a variation of 6 dB over ±2 counts of FDAC.

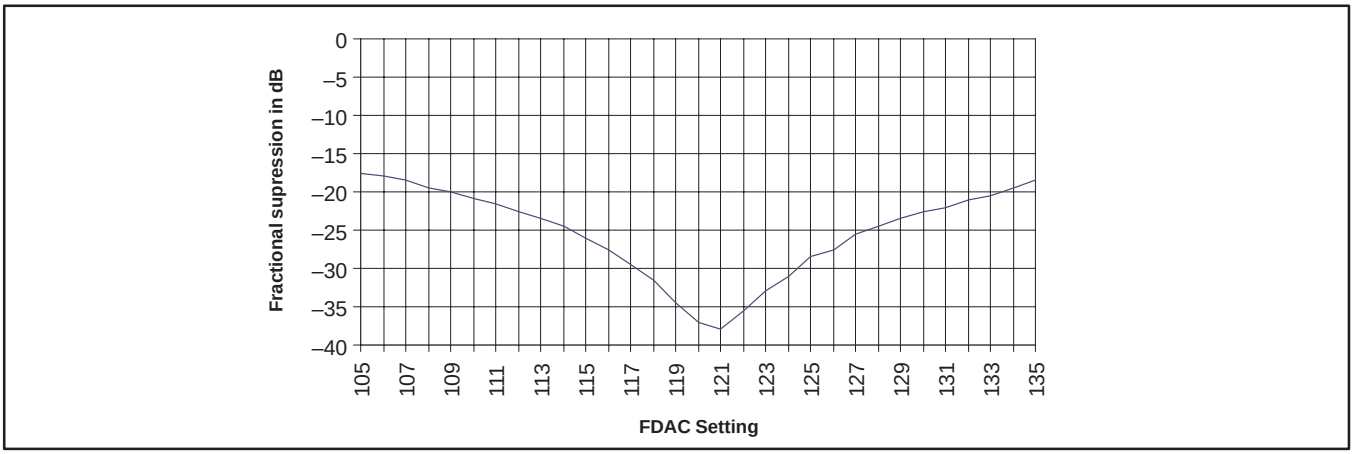


Figure 5. Typical fractional spur levels vs. FDAC setting.

Although it is desirable to have the fractional compensation remain constant over frequency, there will always be variations to work with. If these variations are a problem, the designer may have to create a look–up table of FDAC values to invoke at various points across the frequency band of the target application.

Figure 6 shows the variation in fractional compensation referenced to the carrier across a 150 MHz frequency band with I_{set} = 163 µA, V_{DD} = 3 V, NF = 1 and FDAC = 119.

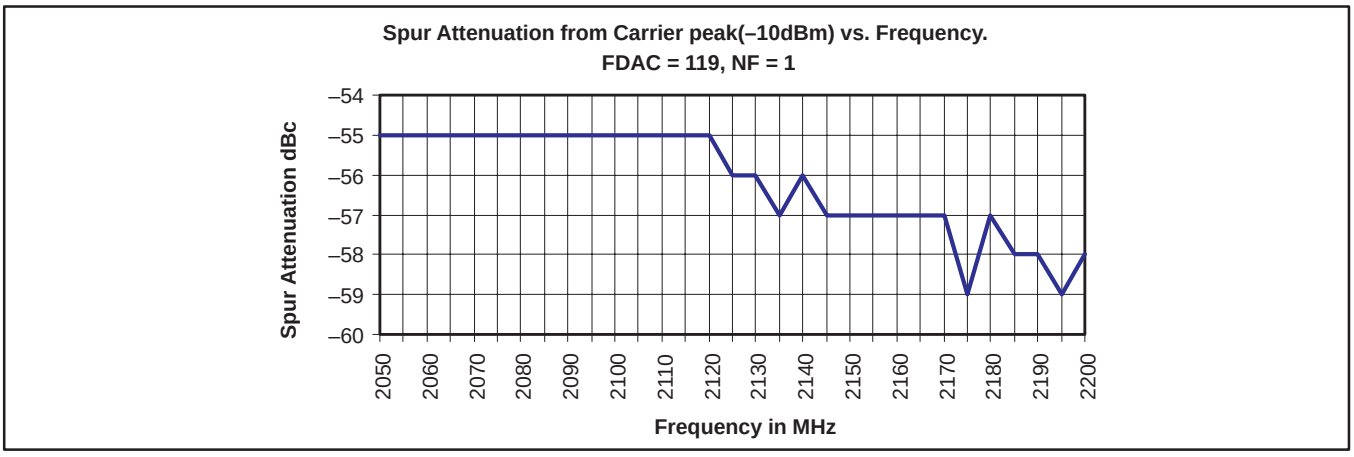


Figure 6. Typical variation in fractional compensation referenced to carrier level.

Figure 7 shows the relative spur attenuation referenced to the worst case FDAC = 0. FDAC = 119 was determined to be the optimum setting for I_{set} = 163 µA, V_{DD} = 3 V, and NF = 1.

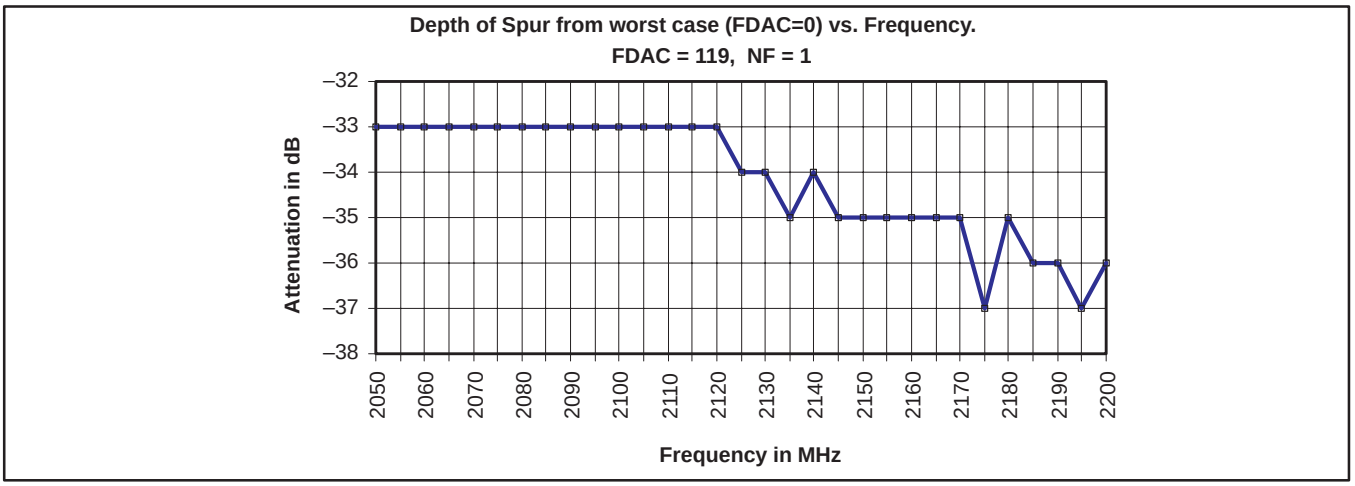


Figure 7. Typical spur attenuation over frequency.

3.3 The secondary glitch

The charge pumps enter the speed-up mode (high gain mode) on the rising edge of the strobe, after the last bit of the A word is sent. The charge pumps will go back to normal mode when the strobe returns to the low state. The width of the strobe pulse should be adjusted to be less than the settling time of the filter, minus the settling time of the glitch in order to allow the filter to settle quickly.

The secondary glitch is caused by the charge pump returning from the higher current speed-up mode to the lower current normal mode (effectively the closed loop environment is changing). The switching of modes causes a difference in final phase error due to a change in the current gain of the charge pumps. This results in a small frequency jump or “glitch” in the time domain. The glitch will cause a phase error and extend the settling time by the width of the glitch. The frequency pulling due to the glitch is dependent upon the loop filter design. In Figure 8 a frequency pull of 23 kHz is observed with a loop filter targeting the GSM application, i.e. a fairly wide loop bandwidth in order to achieve <200 μs switching speeds.

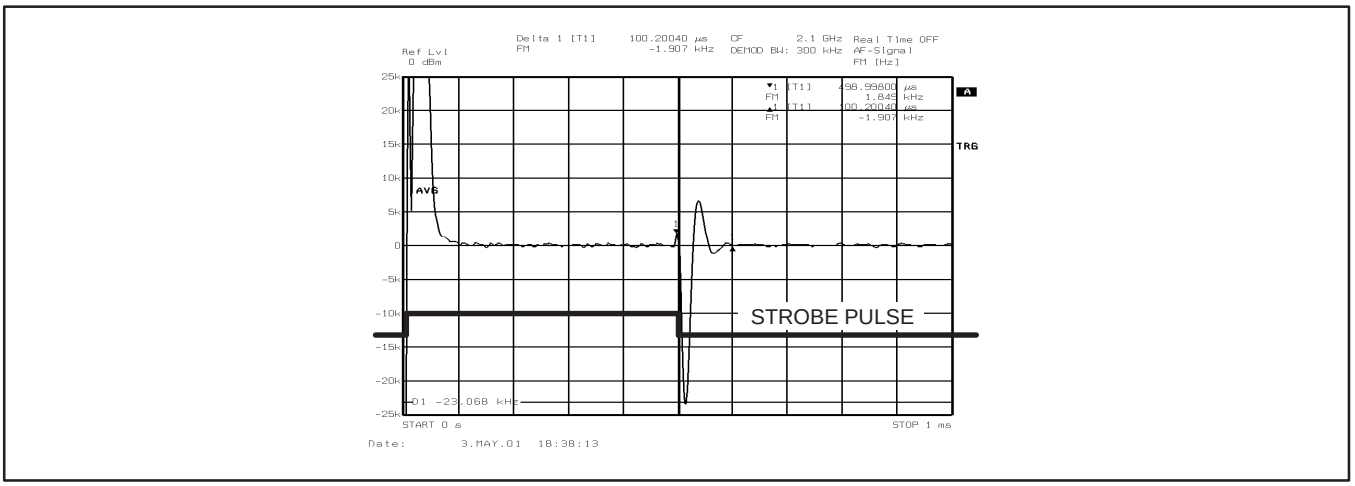


Figure 8. Secondary glitch with GSM loop filter ... frequency pull, 23 kHz typ.

In Figure 9 a frequency pull of 10 kHz is observed for the narrower loop filter design targeting the TDMA application, i.e. ~1.5 ms switching speed.

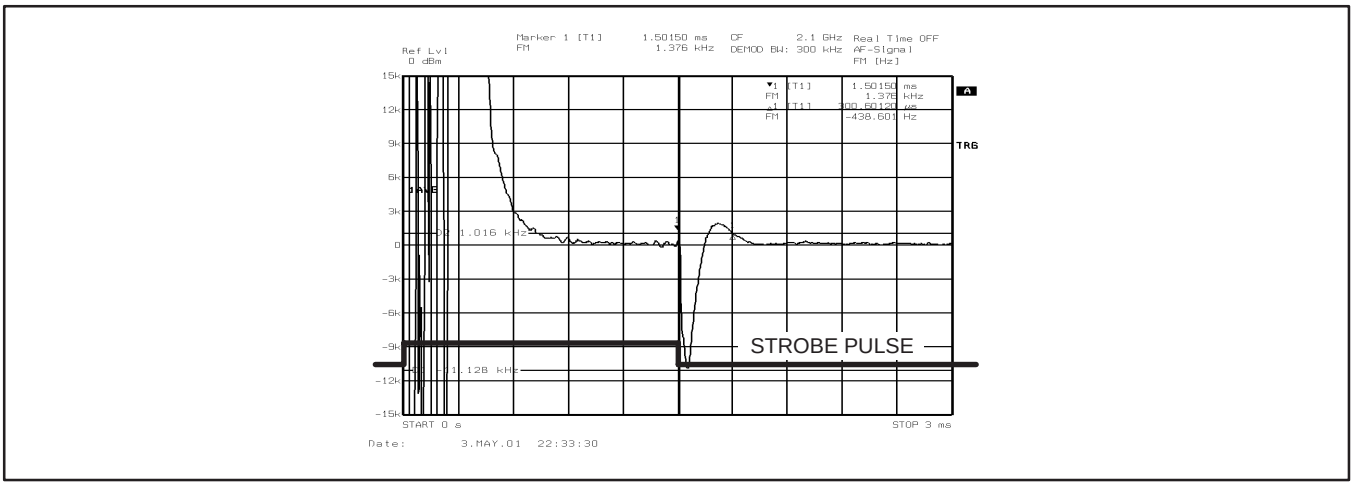


Figure 9. Secondary glitch with TDMA loop filter ... frequency pull, 10 kHz typ.

3.4 Programming sequence

Figure 10 depicts the proper programming sequence for the SA8027.

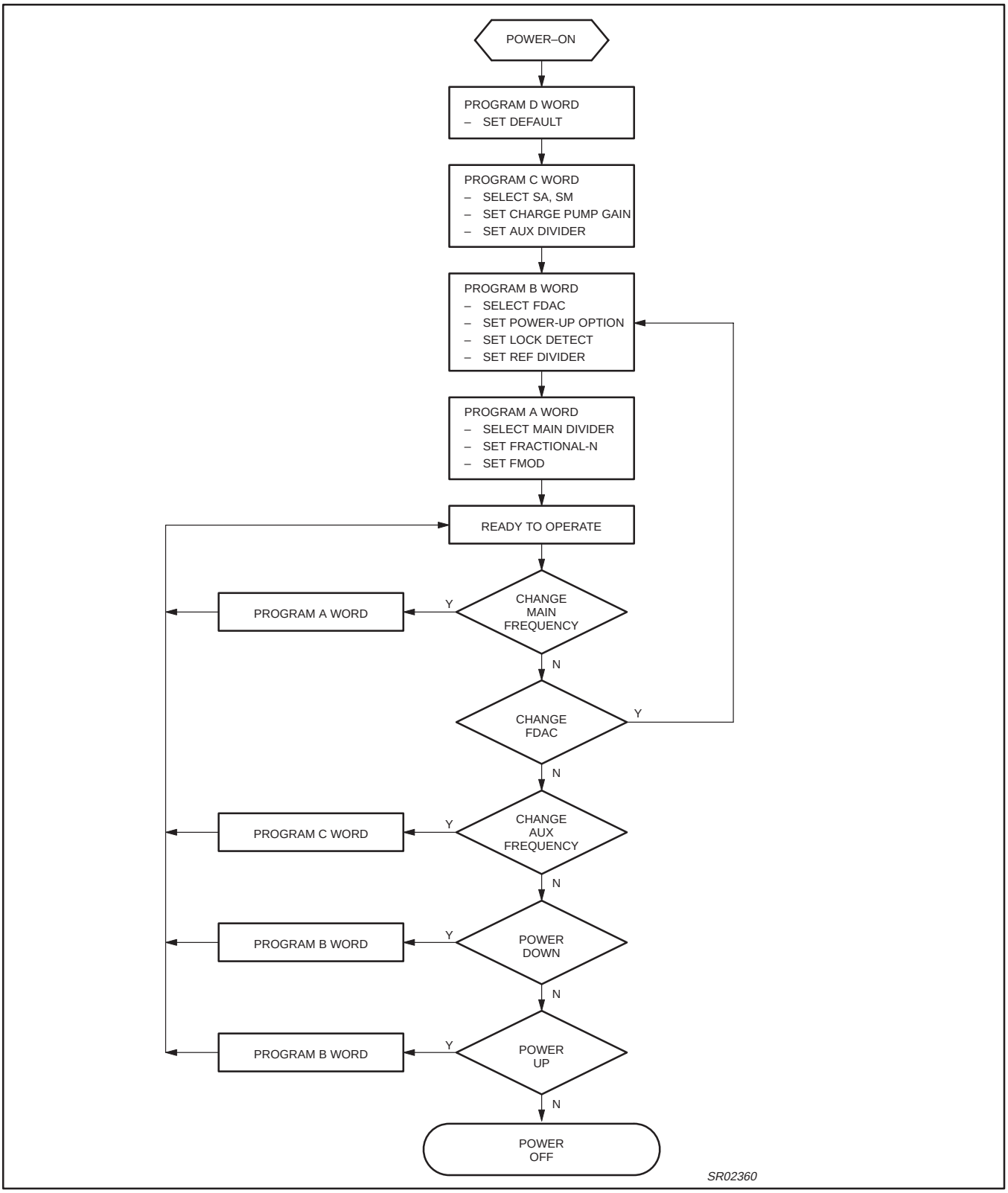


Figure 10. Flow diagram for properly programming the SA8027.

3.4.1 The SA8027 control words

The SA8027 has four programmable words labeled A through D. The initial programming of the device must start with the D word and progress to the A word. The D word is used primarily for Philips internal test purposes and may need to be initially cleared (loaded with “all–zeroes”) to assure that these register bits are in a state that allows the device to function normally.

3.4.1.1 D word

It is recommended to clear this register upon power up to protect against unintentional transient/spurious programming. Once cleared there will normally be no need to write to this register again. This D word has two user bits to control the speedup function. The bit labeled **Tspu** when set, will enable the speedup mode at all times, and the bit labeled **Tdis–spu** will disable this mode. On occasion, this register may become corrupted and the device will go into a test mode rendering it unresponsive. This could lead to a false conclusion that the part is not working or latched–up. If this should occur, the D word will have to be cleared to restore the SA8027 to normal operation.

3.4.1.2 C word

This word contains the auxiliary divider, charge pump current gain selection and two post reference dividers [“SM” and “SA”]. These dividers are used to further divide the reference frequency before delivery to the phase detectors. The “SM” divider is for the main synthesizer and the “SA” divider for the auxiliary.

3.4.1.3 B word

This word controls the reference divider, selects the lock detect output configuration, and contains the power down control and FDAC controls. Any FDAC value loaded will be held and implemented only after the A word is sent.

It is imperative that the C word and B word be loaded before the main frequency values are sent to the A word, failure to do so will create a non–valid loop control and the loop will not lock. After initialization of these two registers, any change in frequency of the main loop can be done by sending the A word only.

3.4.1.4 A word

The main synthesizer divider is programmed via the A Word. This control word contains the integer part, fractional part and modulus select bit. The SA8027 is designed to select one of two modulus values, either 5 or 8. This modulus value, along with the NF value, will determine the fractional value. Starting with a channel step frequency of 200 kHz and a modulus of 5, will result in a main comparison frequency, F_{comp}, that is the product of the two, i.e. F_{comp} = 200 kHz * 5 = 1 MHz. The fractional part of the divide ratio is determined as follows:

NF is the fractional register value.

F_{mod} = Modulus set to 5.

F_{vco} = Frequency set to 2100.6 MHz.

F_{comp} set to 1 MHz.

(INT) is the integer part rounded down.

$N = (INT)(F_{vco}/F_{comp}) = 2100.6 * 10^6 / 1 * 10^6 = 2100.$

$NF = modulus * (F_{vco}/F_{comp} – N).$

$F_{vco}/F_{comp} = 2100.6/1 = 2100.6.$

Subtracting the integer part (N) of 2100 leaves the decimal 0.6. Multiplying by the selected modulus of 5 yields: 5 * 0.6 = 3. The A word can now be loaded with N = 2100, NF = 3, and F_{mod} = 5 to obtain the desired VCO frequency of 2100.6 MHz.

Frequency steps will be accomplished by stepping the fractional register until the maximum count of NF = FMOD – 1 is reached. The next increment will be interpreted as over flow. The NF register is reset to zero and the integer register incremented for the next frequency increment.

Since any changes made to FDAC take affect only after the A word has been sent, the B word must precede the A word for proper operation. Refer to the data sheet for the bit mapping of the A, B, C and D words.

3.4.2 3-Wire Bus relationships

Figure 11 is an abbreviated diagram showing the relative timing of the data, clock and strobe pulses. Note that the strobe pulse is shown as a narrow pulse for all words except the A word. The strobe pulse following the A word is shown wider to indicate that the strobe width has been adjusted to obtain the best settling time of the loop filter. As previously mentioned, after initialization any change in frequency can then be achieved by sending only the A word.

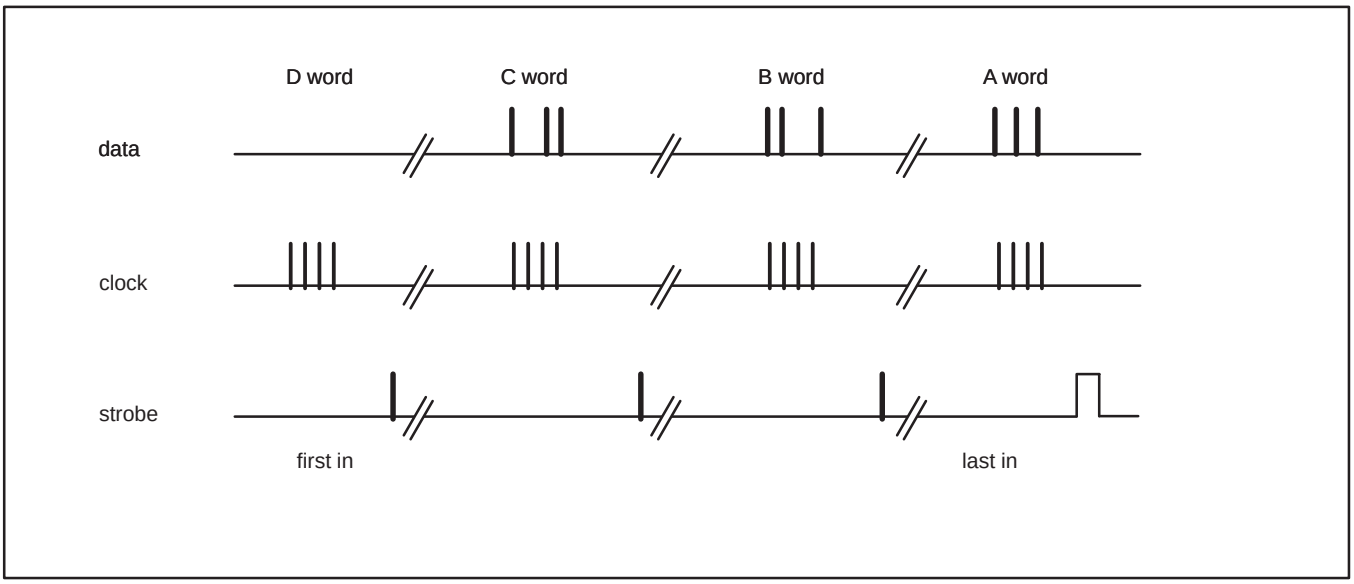


Figure 11. Abbreviated view of the 3-wire bus data stream.

Figure 12 is a more detailed view of the data stream showing the last two words sent out during the initialization of the device. Again, the B word has a narrow strobe while the A word shows a strobe that has been adjusted to optimize the settling time of the filter.

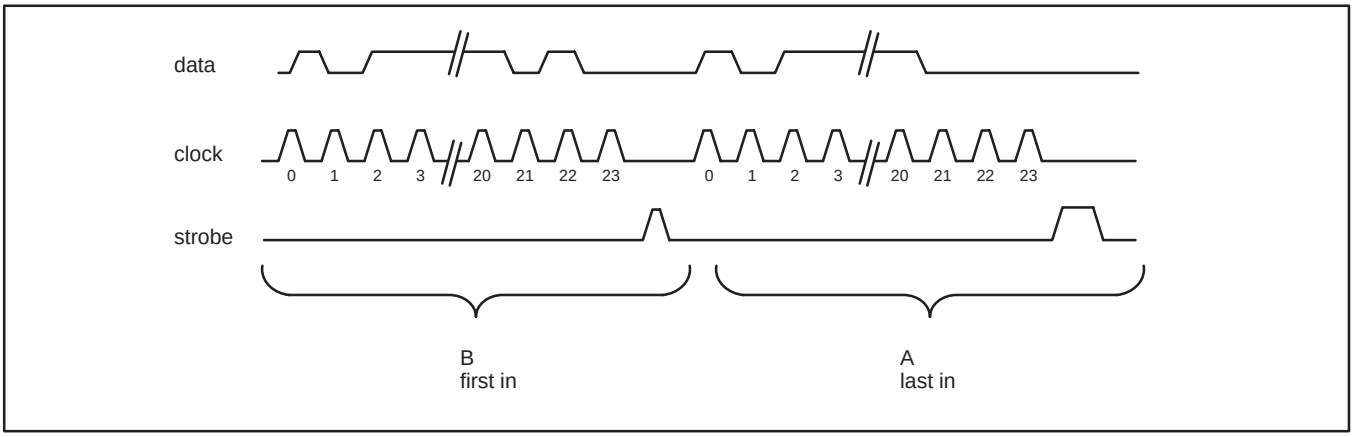


Figure 12. Expanded data stream.

3.5 Main synthesizer speedup mode

In the speedup mode the charge pump sinks/sources additional current to/from the loop filter to reduce the switching time, while normal mode offers the lowest phase noise. The loop filter is charged/discharged faster by increasing the charge pump gain when making large frequency steps. The strobe pulse has multiple functions; first, to latch data on the leading edge of the pulse, and second, to enable and disable the speedup mode. The speedup mode is active as long as the strobe line is held in the high state after latching in the data for the A word. Figure 13 shows the pump current as they relate to the strobe pulse and I_{set} for CP = 00. The CP register bits in the C word select the gain for the charge pumps as a multiple of the reference current (I_{set}) which in turn is set via an external resistor, R_{set}.

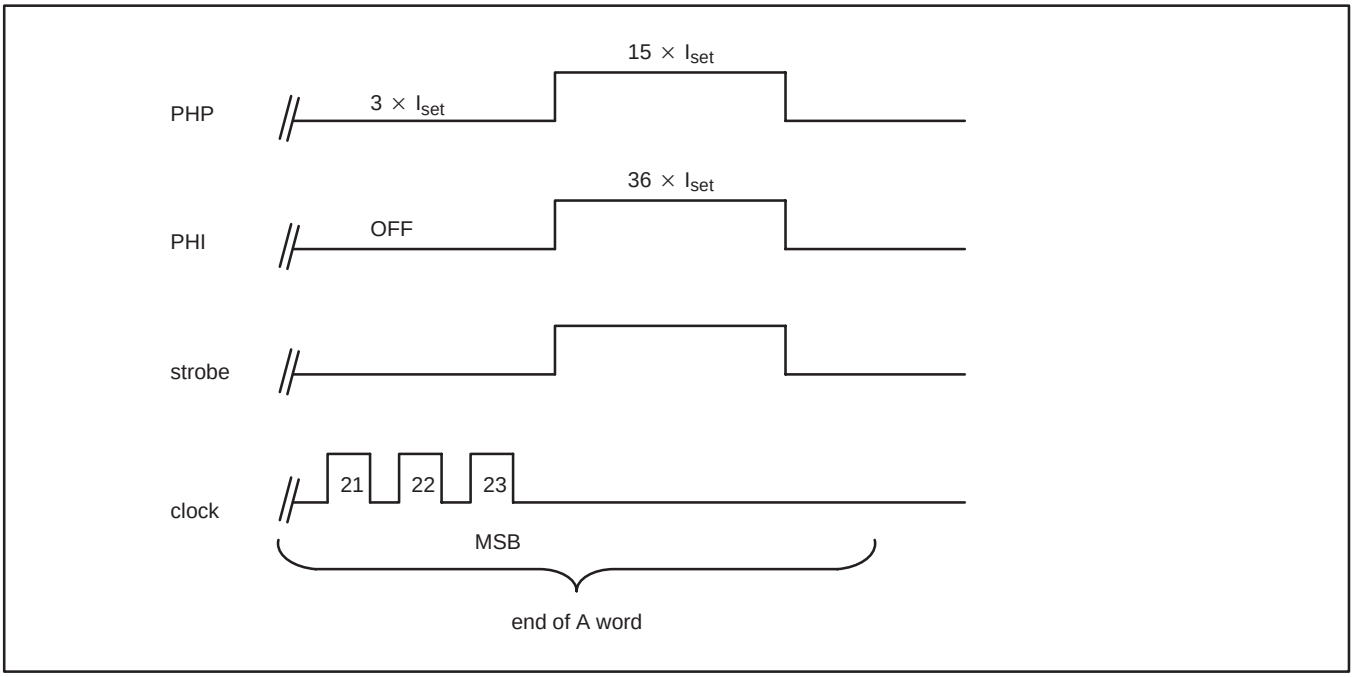


Figure 13. Pump currents related to the strobe pulse.

3.6 Phase detector and charge pumps

The main phase detector drives two charge pumps PHP and PHI while the Aux phase detector drives the PHA charge pump. The charge pump currents are set via software and external resistor R_{set}.

The PHI pin is used to furnish a higher current directly to C1, as shown in Figure 14. This pin can furnish a current up to 36 times I_{set} or 6 mA with I_{set} set to 163 μA in order to charge C1 faster to reduce switching time. It is not recommended to connect the PHI pin directly to PHP as this will not offer as much improvement in switching speed as when connected directly to C1 as shown in Figure 14.

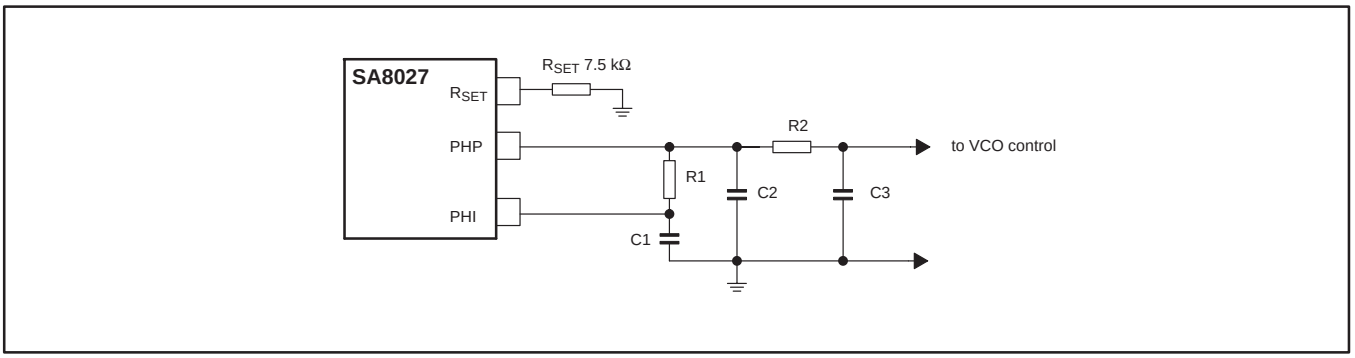


Figure 14. PHI connection.

3.6.1 Charge pump current setting

Table 1 shows how the main and auxiliary charge pump currents can be adjusted via the CP register bits. The reference current I_{set} is set by an external resistor R_{set}. By design, R_{set} should be chosen to be between 6 kΩ and 15 kΩ.

$$I_{set} = \frac{V_{set}}{R_{set}}$$ where V_{set} is a regulated reference voltage of 1.22 V.

Table 1. Charge pump current settings

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI}
0	0	$1.5 \times I_{set}$	$3 \times I_{set}$	$15 \times I_{set}$	$36 \times I_{set}$
0	1	$0.5 \times I_{set}$	$1 \times I_{set}$	$5 \times I_{set}$	$12 \times I_{set}$
1	0	$1.5 \times I_{set}$	$3 \times I_{set}$	$15 \times I_{set}$	OFF
1	1	$0.5 \times I_{set}$	$1 \times I_{set}$	$5 \times I_{set}$	OFF

Table 2 shows how the pump currents will vary with different settings of the CP register for R_{set} = 7.5 kΩ which results in an I_{set} = 164 μA.

Table 2. Selecting charge pump currents with register CP

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI}
0	0	246 μA	492 μA	2.46 mA	5.9 mA
0	1	82 μA	164 μA	820 μA	1.97 mA
1	0	246 μA	492 μA	2.46 mA	0
1	1	82 μA	164 μA	820 μA	0

3.7 RF/Main divider

The RFin differential inputs drive a pre-amplifier to provide the clock for the RF/main divider. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. Figure 15 is the graphical representation and Table 3 a tableized listing of the RF input impedance measured directly at the pin of the device for V_{DD} = 3 V. For single-ended operation, the input signal should be AC coupled to one of the inputs while the other input pin is AC grounded. The divider consists of a fully programmable bipolar prescaler (first 7 bits) followed by a CMOS counter. Total divide ratio range is from 512 to 65535.

At the completion of the RF/main divider cycle, an output pulse is generated that drives the main phase comparator and the fractional accumulator. The fractional accumulator is incremented by the value of NF whenever the RF/main divider completes a cycle. Whenever the fractional accumulator overflows, the RF/main divider division ratio will be increased by 1 to N+1, resulting in an average division ratio of N + NF/FMOD.

The output of the RF/main divider will be modulated with fractional jitter. This phase jitter is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

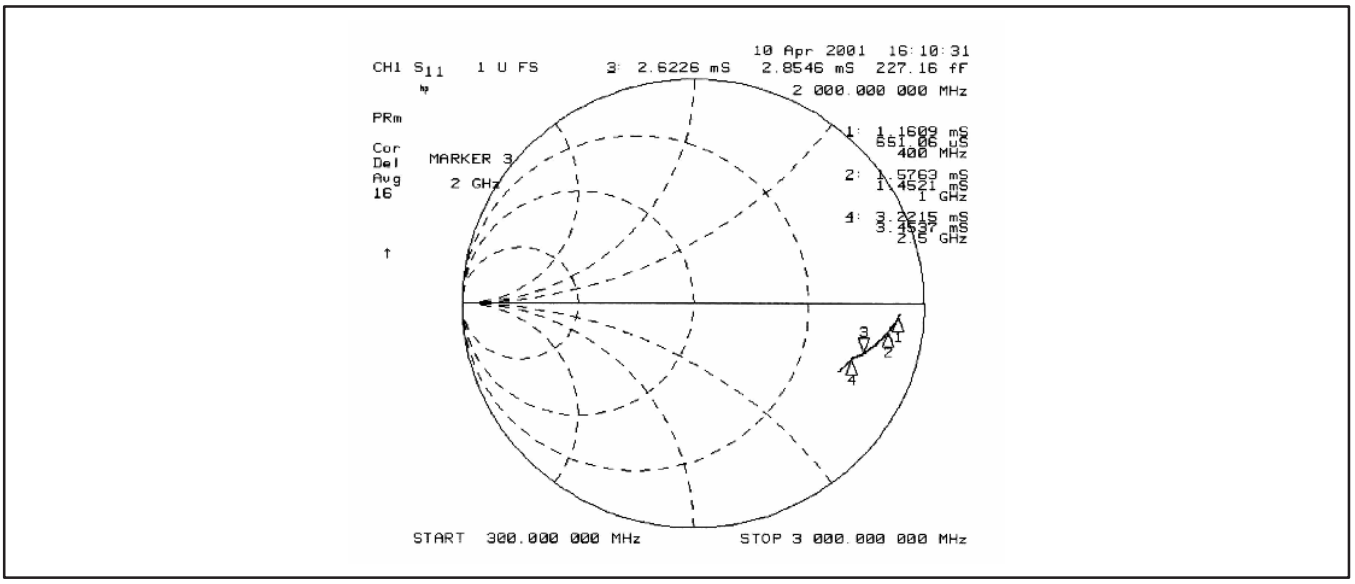


Figure 15. Typical RF/Main input impedance, V_{DD} = 3 V.

Table 3. Typical RF/Main divider input impedance, V_{DD} = 3 V

Frequency (MHz)	Mag	Angle
300	8.898	–2.832
400	0.893	–3.489
500	0.888	–4.181
600	0.883	–4.924
700	0.877	–5.630
800	0.872	–6.336
900	0.866	–7.063
1000	0.859	–7.776
1100	0.853	–8.556
1200	0.846	–9.284
1300	0.839	–10.066
1400	0.832	–10.826
1500	0.824	–11.605
1600	0.817	–12.433
1700	0.810	–13.210
1800	0.802	–14.045
1900	0.794	–14.851
2000	0.786	–15.589
2100	0.777	–16.369
2200	0.769	–17.045
2300	0.760	–17.637
2400	0.752	–18.152
2500	0.746	–18.674

Figure 16 shows the typical RF/Main divider Input Sensitivity vs. Frequency and Supply Voltage. Temp = 25 °C; I_{SET} = 164 µA; NF = 0; FMOD = 8; N = 853.

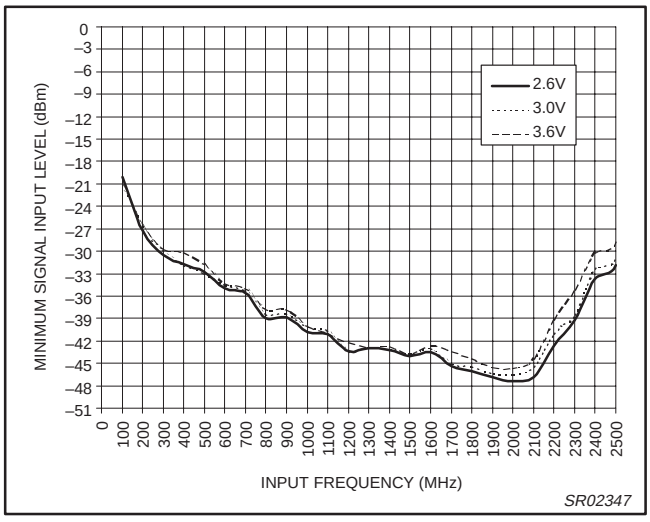


Figure 16. Typical main divider input sensitivity.

3.8 Reference divider

The reference oscillator drives a preamplifier to provide the clock for the reference divider. The maximum frequency allowed is 40 MHz. For best noise performance, it is recommended that a TCXO be used. The reference divider can be programmed with values between 4 and 1023 and is followed by a three-bit binary counter. The 3-bit SM counter for the RF and 3-bit SA counter for the IF synthesizer, determines which of the 5 output pulses are fed to the phase detector inputs (refer to Figure 1). To avoid cross talk between the main and auxiliary divider, the phase detector signals generated by the reference divider for the main phase detector occur at a different time as those for the auxiliary divider. Figure 17 is a graphical representation and Table 4 a tableized listing of the typical reference input impedance for V_{DD} = 3 V.

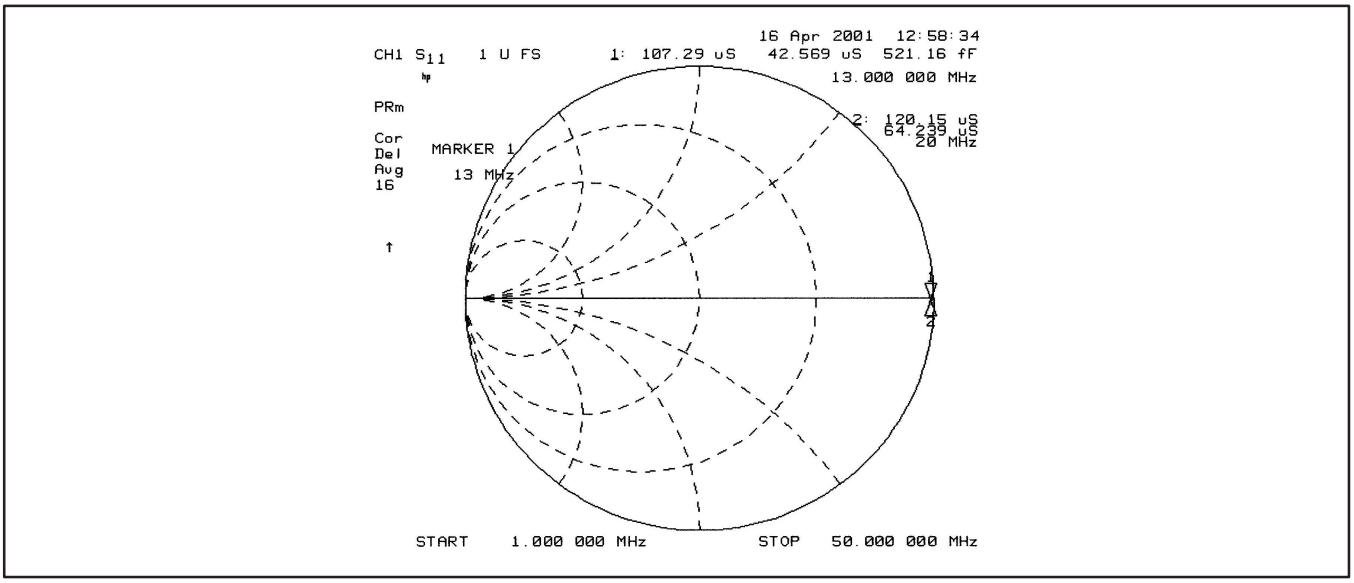


Figure 17. Typical reference input impedance, V_{DD} = 3 V.

Table 4. Typical reference divider input impedance, V_{DD} = 3 V

Frequency (MHz)	Mag	Angle
5	0.991	–0.048
10	0.991	–0.083
15	0.991	–0.090
20	0.991	–0.134
25	0.991	–0.168
30	0.990	–0.208
35	0.990	–0.238
40	0.990	–0.258
45	0.990	–0.281
50	0.990	–0.316
55	0.990	–0.348
60	0.989	–0.371
65	0.989	–0.394
70	0.989	–0.417
75	0.989	–0.449
80	0.989	–0.470
85	0.989	–0.493
90	0.988	–0.522
95	0.988	–0.549
100	0.988	–0.579

Figure 18 shows the typical reference divider input sensitivity vs. frequency and supply voltage. Temp = 25 °C; I_{SET} = 164 µA; Divider Ratio = 682.

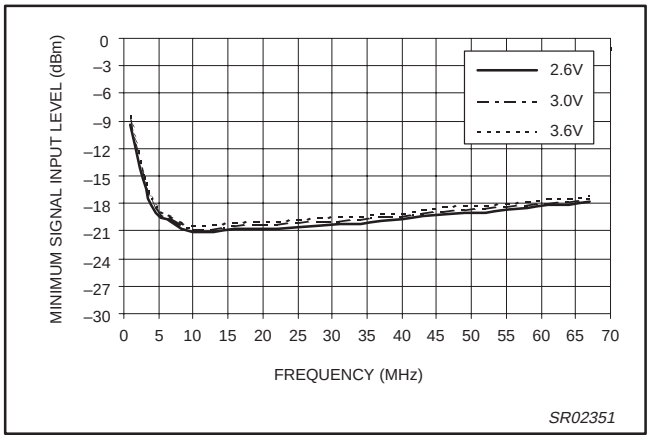


Figure 18. Typical reference divider input sensitivity.

3.9 IF/Auxiliary divider

The IF/auxiliary divider structure is the same as that of the main, except that there is no fractional capability and it is only a 14–bit divider. Permissible divide ratios range from 128 to 16383.

Figure 19 is the graphical representation and Table 5 a tabelized listing of the typical input impedance of this port for V_{DD} = 3 V.

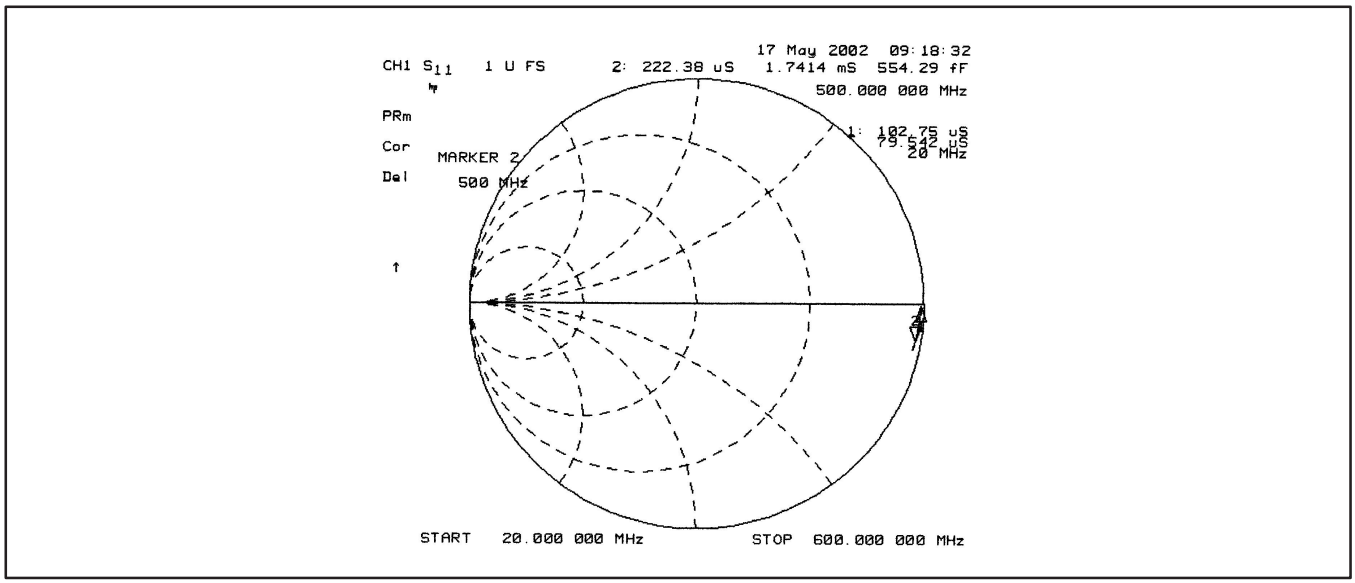


Figure 19. Typical IF/Aux input impedance, V_{DD} = 3 V.

Table 5. Typical IF/Auxiliary divider input impedance, V_{DD} = 3 V

Frequency (MHz)	Mag	Angle
20	0.99	–0.2
40	0.99	–0.4
60	0.99	–0.5
80	0.99	–0.6
100	0.99	–0.8
120	0.99	–0.9
140	0.99	–1.0
160	0.99	–1.1
180	0.99	–1.2
200	0.99	–1.3
220	0.99	–1.5
240	0.99	–1.6
260	0.98	–1.7
280	0.98	–1.8
300	0.98	–1.9
320	0.98	–2.1
340	0.98	–2.2
360	0.98	–2.4
380	0.98	–2.5
400	0.98	–2.6
420	0.98	–2.7
440	0.98	–2.7
460	0.98	–2.9
480	0.98	–3.0
500	0.98	–3.1
520	0.98	–3.2

Figure 20 is the typical IF/Auxiliary divider input sensitivity vs. frequency and supply voltage. Temp = 25 °C; I_{SET} = 164 µA; Divider Ratio = 213.

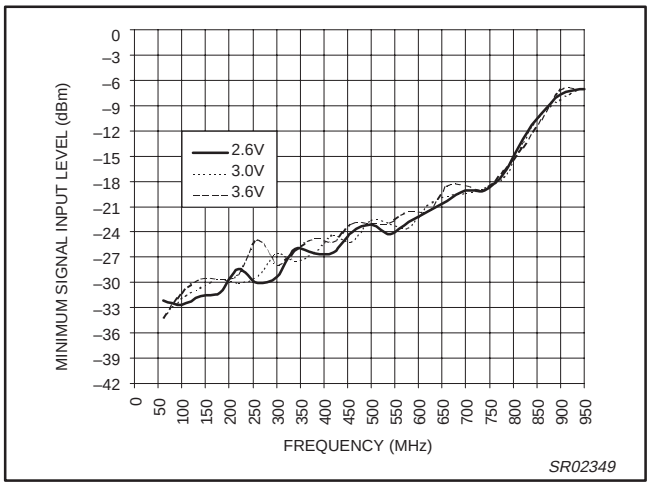


Figure 20. Typical auxiliary divider input sensitivity.

3.10 Lock detect

There are four states that the lock detect output can be placed in. The first selects a configuration where the lock detect output is set for active pull up for both Main and Aux while the second is selected as open drain for both Main and Aux. The last two states are independent functions where the third selects the main synthesizer lock detect only and the fourth selects the auxiliary lock detect only. The output LOCK maintains a logic ‘1’ unless the auxiliary phase detector or the main phase detector is out of lock. The lock condition for the main and the auxiliary synthesizers are defined as a phase difference of less than 1 period of the reference frequency.

3.11 Power down

The device can be powered down by hardware or software. The PON (hardware) signal is exclusively ORed with the PD (software) bits in the B word. If PON = 0, then the part is powered up when PD = 1. When the synthesizer is reactivated from power down, the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

3.12 Test pin

The Test pin is used as an input pin for the test mode. For normal operation of the synthesizer, this pin should be either grounded or connected to V_{DD}.

4.0 Loop filter design equations

$$\delta = \frac{\textit{frequency error after settling}}{\textit{switching step}} \qquad \textbf{Equation (1)}$$

t_{sw} : Switching time (sec)
f_n : Natural frequency (Hz)
ω_n : $2\pi f_n$ (rad/sec)
N : Divide ratio
ζ : Damping factor
K_{VCO} : VCO gain (rad/V) = 2π VCO gain (Hz/V)
K_Φ : Phase detector gain = $I_{CP}/2\pi$ (A/rad)

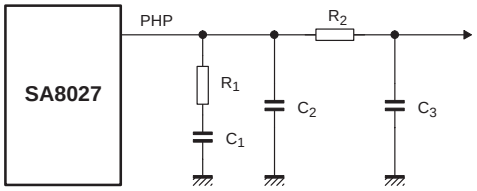
$$\omega_n = \frac{-\ln\left(\delta \cdot \sqrt{1-\zeta^2}\right)}{\zeta \cdot t_{sw}} \qquad \textbf{Equation (2)}$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N \cdot \omega_n{}^2} \qquad \textbf{Equation (3)}$$

$$R_1 = 2 \cdot \zeta \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \qquad \textbf{Equation (4)}$$

$$C_2 \leq \frac{C_1}{10} \qquad \textbf{Equation (5)}$$

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_n \qquad \textbf{Equation (6)}$$



$$BW_{3dB} = \frac{\omega_n}{2\pi}\left[2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}\right]^{1/2} \qquad \textbf{Equation (7)}$$

4.1 RF/Main loop filter design example for the GSM application

VCO frequency (F_{VCO}) = 2083 to 2108 MHz
Channel spacing (F_{chan}) = 200 kHz
Comparison frequency (F_{comp}) = 5 × 200 kHz = 1 MHz
Switching time (t_{SW}) = 180 µs
Switching step = 25 MHz
Frequency error = within 200 Hz
VCO gain (K_{VCO}) = 65 MHz/V Murata MQG101-2100
Reference crystal (F_{REF}) = 13 MHz
V_{set} = 1.22 Volts

Determine R_{set}

Choose I_{CP} = 500 = 500 µA; CP = 00 = a gain of 3 (see Table 1)

$$R_{set} = \frac{3 * V_{set}}{I_{CP}} = \frac{3.66}{500 * 10^{-6}} = 7.32\ k\Omega \quad \Rightarrow \text{use } 7.5\ \text{k}\Omega$$

$$I_{CP} = 3 * I_{set} = \frac{3 * V_{set}}{R_{set}} = \frac{3.66}{7.5 * 10^{3}} = 488\ mA$$

Determine N

The divide ratio at band center for the VCO is typically used.

$$N = \frac{2100\ MHz}{1\ MHz} = 2100$$

Determine ω_n

From Equation (1):

$$\delta = \frac{200}{25 * 10^{6}} = 8 * 10^{-6}$$

Pick ζ = 0.707 ... critically damped

From Equation (2):

$$\omega_n = \frac{-1_n\left(0.8 * 10^{-6} * \sqrt{1 - 0.707^2}\right)}{0.707 * 180 * 10^{-6}} = 94943 rad/s$$

Determine R_1, C_1, C_2

Using Equation (3) with 2π from K_{VCO} (rad/V) and $^1/_2\pi$ from K_ϕ (A/rad) cancelling out,

$$C_1 = \frac{488 * 10^{-6} * 65}{2100 * 94943^2} = 1.67\ nF \quad \Rightarrow \text{use } 1.5\ \text{nF}$$

using Equation (4)

$$R_1 = 2 * 0.707 * \left(\frac{2100}{488 * 10^{-6} * 65 * 10^{-6} * 1.67 * 10^{-9}}\right)^{0.5} = 8.9\ k\Omega \quad \Rightarrow \text{use } 9.1\ \text{k}\Omega$$

using Equation (5)

$$C_2 = \frac{1.5 * 10^{-9}}{10} = 150\ pF$$

NOTE: The values of C_1 and C_2 used on the demoboard are 680 pF and 56 pF, respectively, which were determined to provide optimum switching performance.

5.0 Typical performance

5.1 Main synthesizer performance for the GSM application

5.1.1 Phase Noise

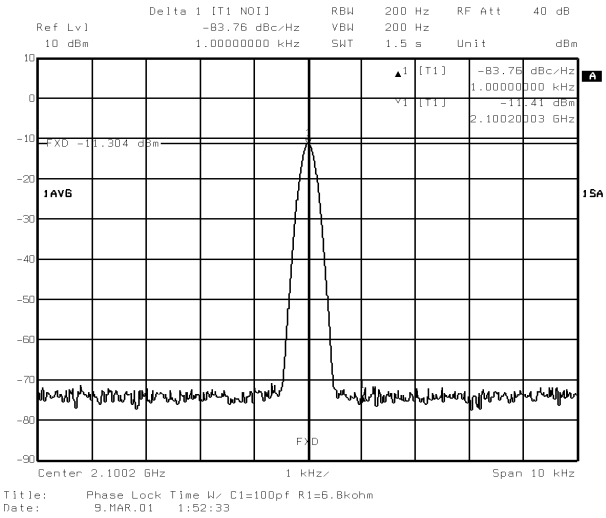


Figure 21. Main synthesizer phase noise at 1 kHz offset, –83.8 dBc/Hz typ.

Figure 22 shows the typical main phase noise measured from 100 Hz to 1 MHz. At 1 kHz offset the marker is measuring a phase noise of *–83.76* dBc/Hz.

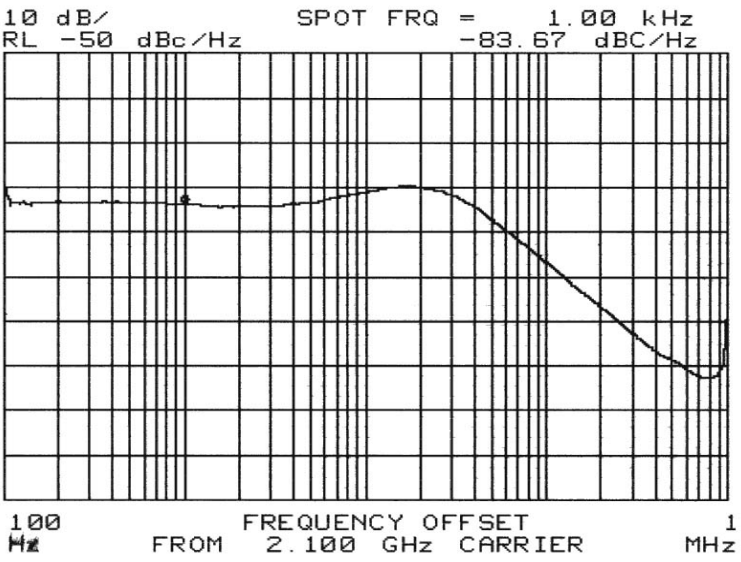


Figure 22. Typical phase noise plot of the main synthesizer

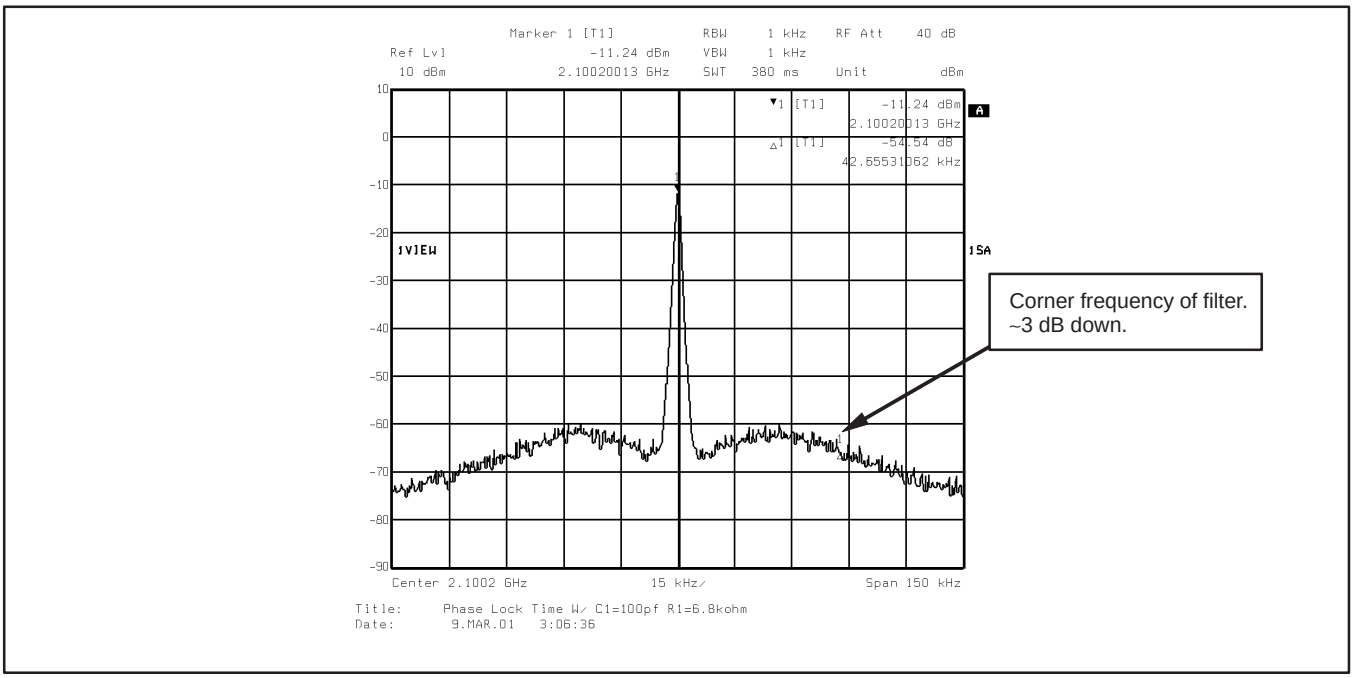


Figure 23. Typical loop filter bandwidthmeasurement of approximately 43 kHz.

Comparison spurs are mainly caused by charge pump mismatch. However, leaky external components, such as loop capacitors and VCO will contribute to this spur.

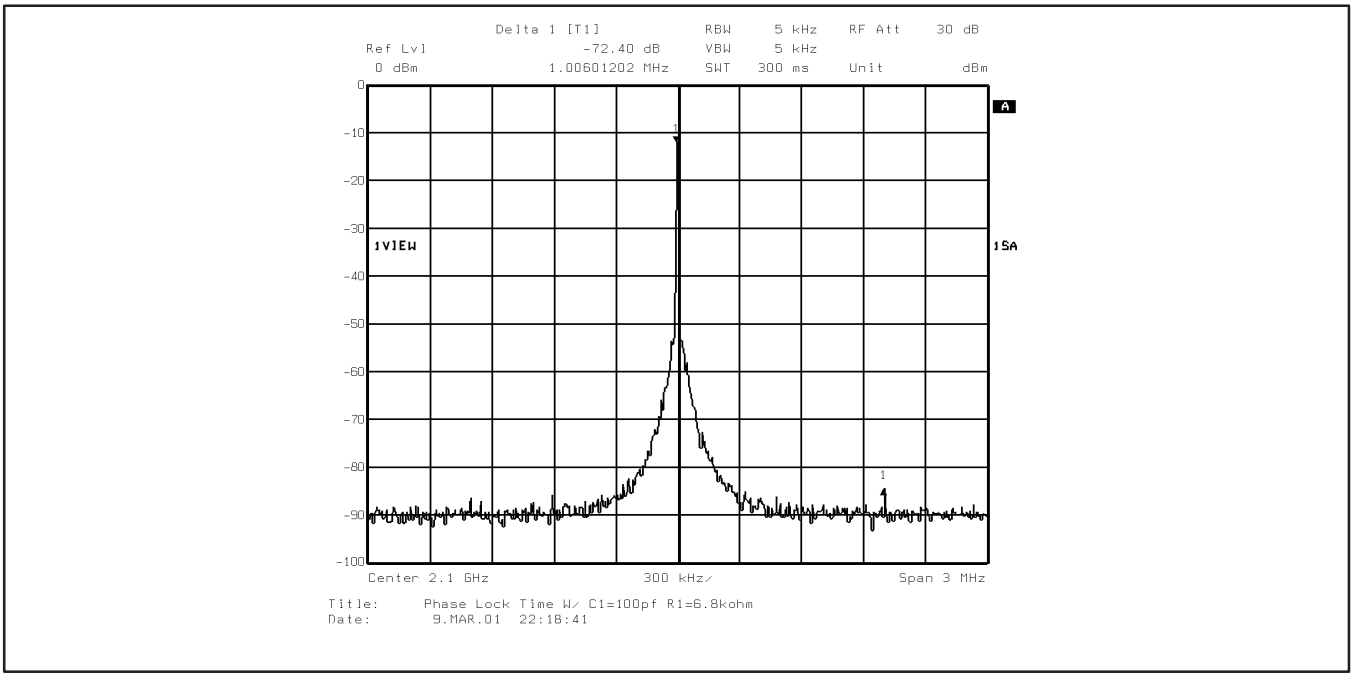


Figure 24. 1 MHz main comparison spur shown to be –72.4 dBc typ.

5.1.2 Switching time

Figure 25 shows connections to the board and to the Rohde and Schwarz FSEM 30 analyzer for making loop filter settling time measurements.

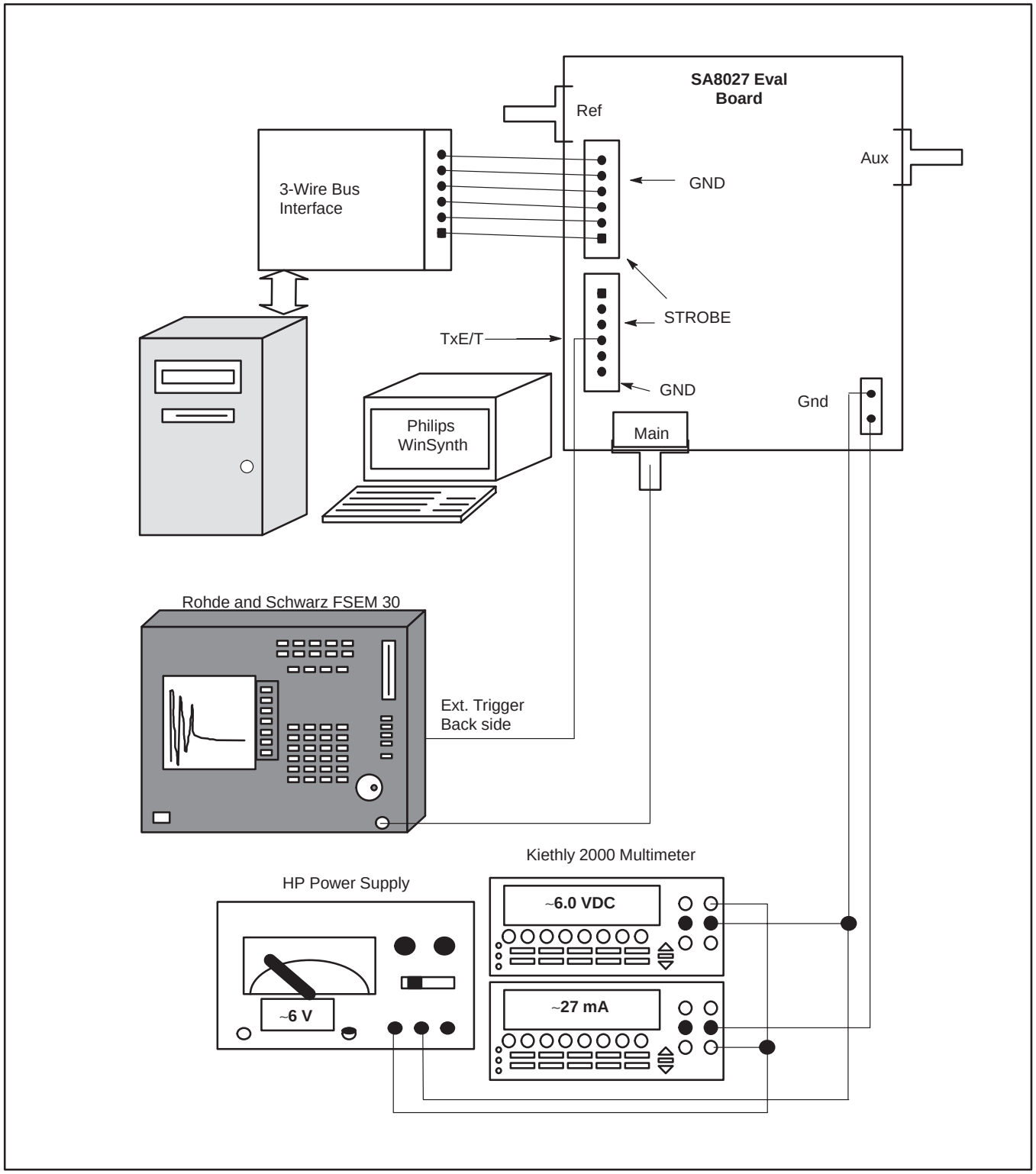


Figure 25. Set-up for measuring loop filter settling time.

The measurement was performed with a Rohde and Schwarz FSEM 30 analyzer configured in vector analyzer mode, analog demod, and FM External triggering. The “Tx En” pin on the evaluation board outputs the trigger pulse that is used to trigger the analyzer on every other strobe pulse.

In the PC control program, the sequencer is loaded with the desired start and target frequencies and “Loop” mode selected so that the sequencer will run continuously, alternating between the two frequencies and triggering the analyzer on the frequency to be measured. The analyzer’s center frequency must be set on the target frequency.

The width of the strobe pulse can be adjusted for the optimum switching time for a given loop filter design. The interrupt driven Windows operating system makes it difficult to make a good measurement of system timing with the PC. The width of the strobe pulse will be close, but will not be the same as that entered in the strobe width control box. Thus, if more accuracy is required, the strobe line should be connected to an oscilloscope and the strobe width adjusted until the required duration is reached.

Figure 26 shows a typical LOW-to-HIGH switching transition to within 200 Hz (25 MHz jump) with a switching time less than 200 μs.

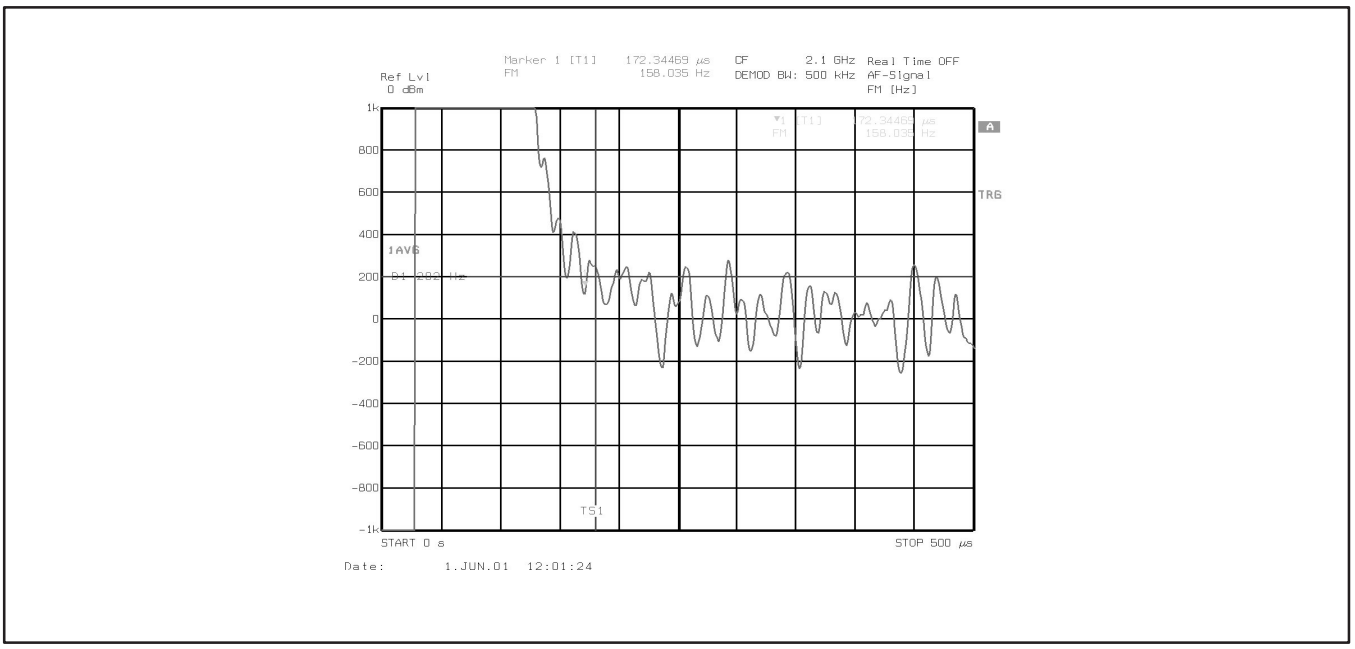


Figure 26. Typical LOW-to-HIGH switching speed transition.

Figure 27 shows a typical HIGH-to-LOW switching transition to within 200 Hz (25 MHz jump) with a switching time less than 200 µs.

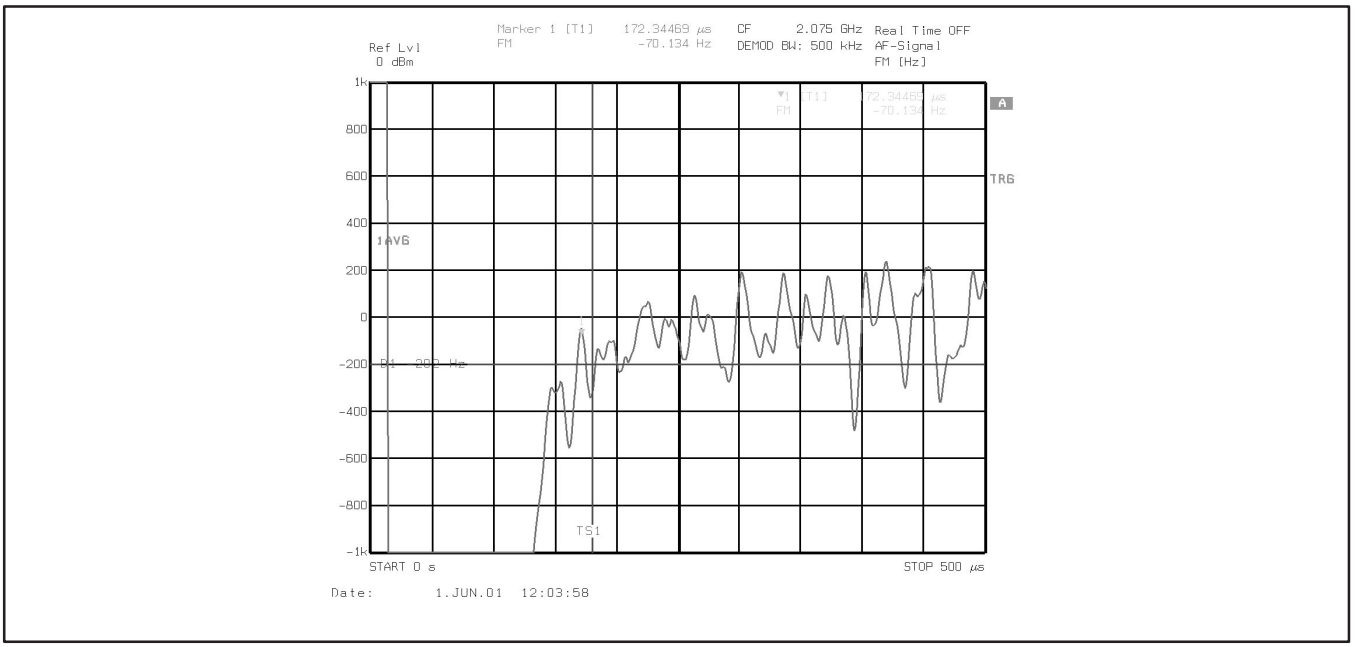


Figure 27. Typical HIGH-to-LOW switching speed transition.

5.2 Auxiliary synthesizer performance

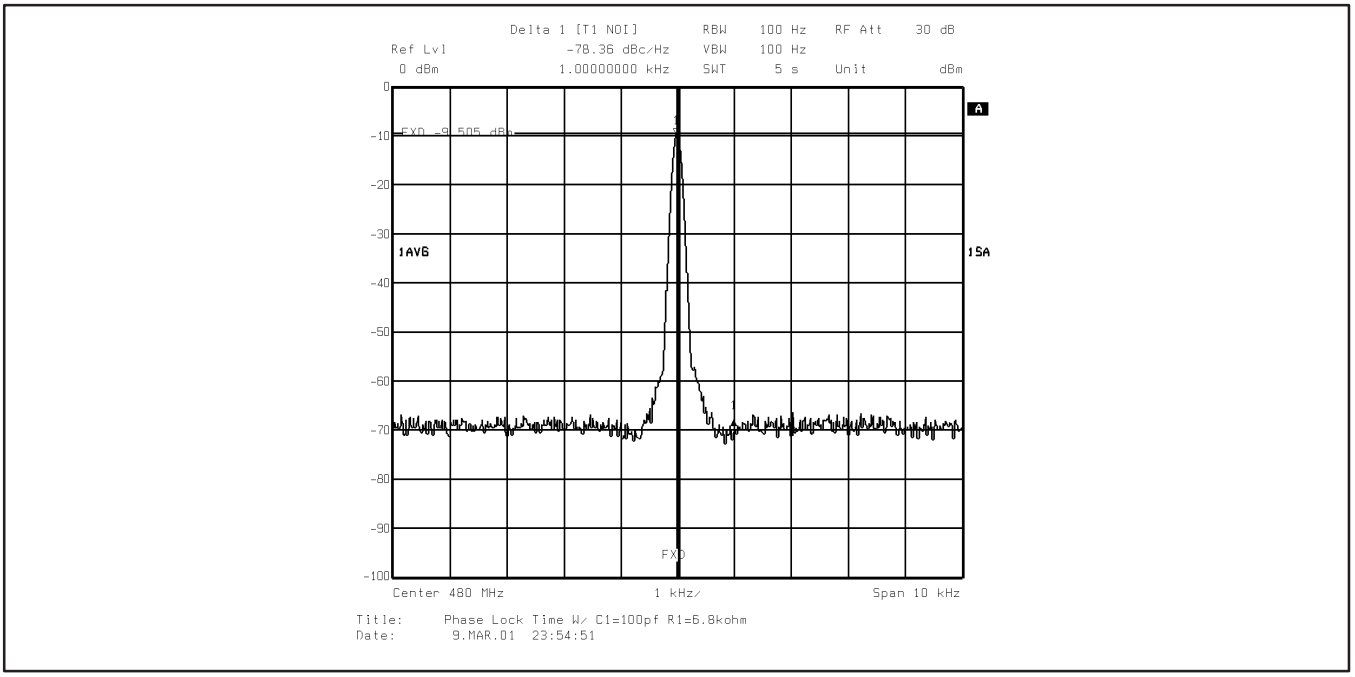


Figure 28. AUX phase noise, measured at 1 kHz offset, is –78.36 dBc/Hz typ.

6.0 Evaluation board set-up

6.1 Set-up

1. Connect the interface cable from the demo board to the interface card.
2. Plug the interface card into the parallel printer port and the six–conductor ribbon cable from the interface card to the evaluation board with the black stripe of the cable on the ground side of the six pin connectors.
3. Supply the demo board with 6 V_{DC}. The board has a 3 volt low drop-out regulator and will draw ~30 mA.
4. Connect MAIN–OUT or AUX–OUT to spectrum analyzer
5. Run “Winsynp1.02.exe” and select SA8027 to program the device.
6. The lock indicator should be OFF when both main and auxiliary synthesizers are in lock.
7. Be sure to set the correct reference frequency in the PC control program.

Supply voltages:

Main VCO : 3.0 V_{DC}
Aux VCO : 3.0 V_{DC}
TCXO : 3.6 V_{DC}

Note: When making spur measurements with a spectrum analyzer you may notice extra signals appearing that are not related to the synthesizer reference or fractional spurs. If this condition is noted, remove the cable from the 6-pin connector on the board. This should eliminate any unwanted signals, that in most cases can be related to a high level signal source on the bench such as the scan rate of the PC monitor or any other type of CRT nearby.

7.0 Evaluation board schematic

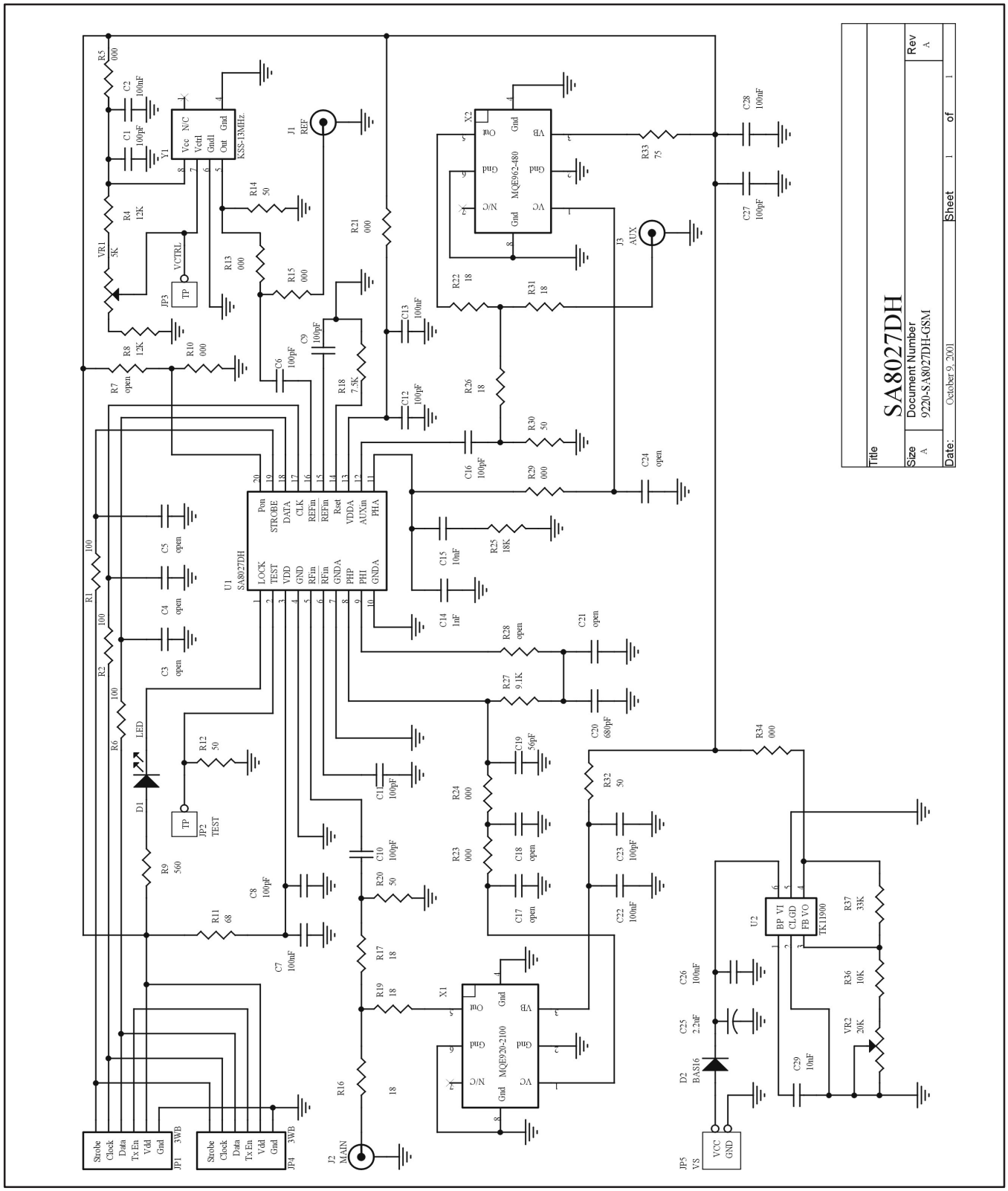


Figure 29. Evaluation board schematic.

8.0 Evaluation board assembly drawing

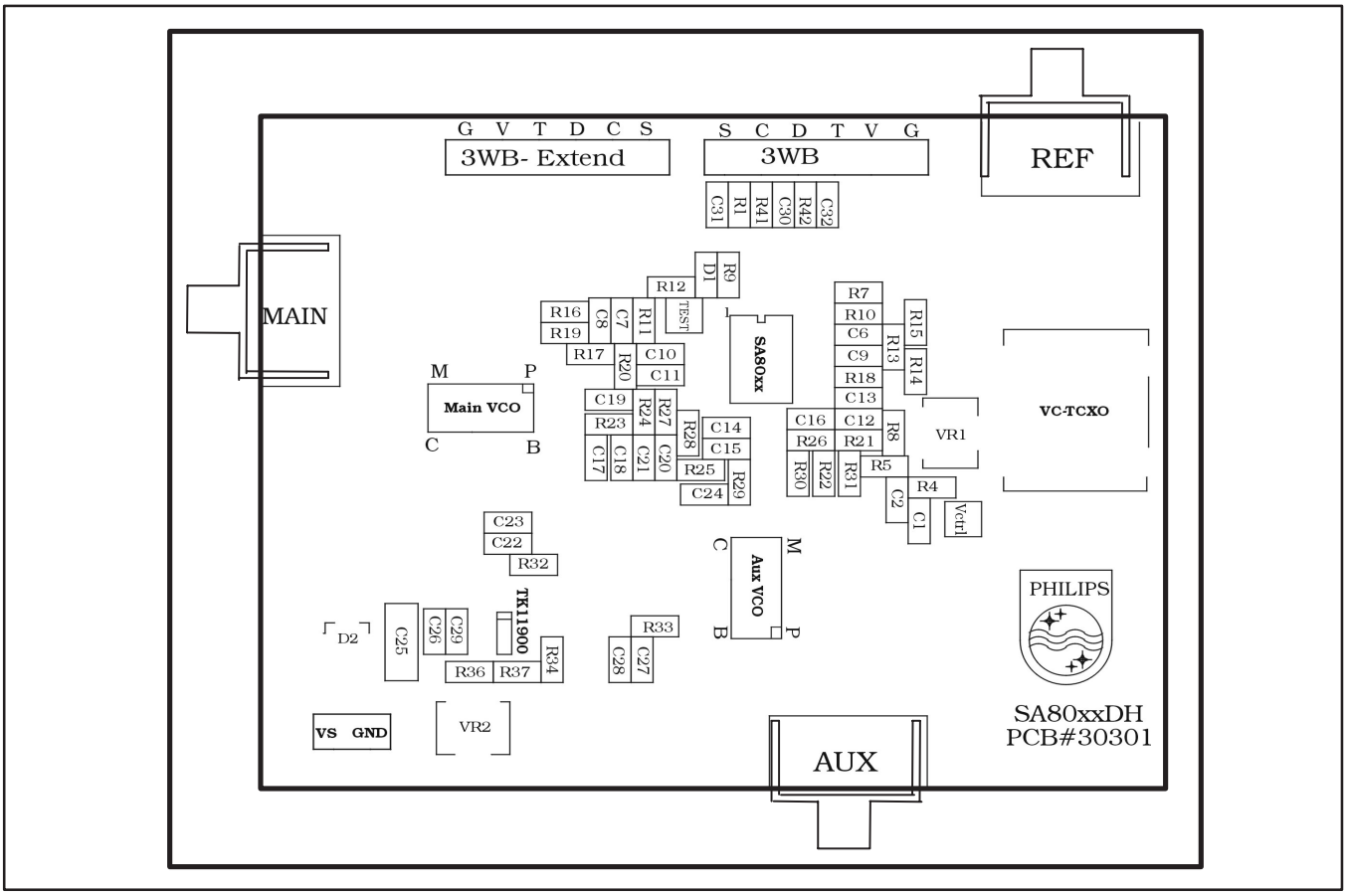


Figure 30. Evaluation board assembly diagram.

9.0 Bill of materials

Qty	Volt	Value	Part reference	Part description	Manufacturer	Part number
				Surface Mount Capacitor		
1	50V	56 pF	C19	CAP CER 0603 NPO ± 5%	PHILIPS	0603CG560J9B20
10	50V	100 pF	C1,C6,C8,C9,C10,C11, C12,C16,C23,C27	CAP CER 0603 NPO ± 5%	PHILIPS	0603CG101J9B20
1	50V	680 pF	C20	CAP CER 0603 NPO ± 5%	PHILIPS	0603CG681J9B20
1	50V	1 nF	C14	CAP CER 0603 X7R ±10%	PHILIPS	06032R102K9B20
2	25V	10 nF	C15,C29	CAP CER 0603 X7R ±10%	PHILIPS	06032R103K8B20
6	25V	100 nF	C2,C7,C13,C22,C26, C28	CAP CER 0603 Y5V ± 20%	PHILIPS	06032F104M8B20
1	10V	2.2 µF	C25	TANTALUM CHIP CAP ± 20%	PANASONIC	ECS–H1AY225R
7		OPEN	C3,C4,C5,C17,C18,C21,C24			
				Surface Mount Resistor		
9		0 Ω	R5,R10,R13,R15,R21, R23,R24,R29,R34	RES CHIP 0603 1/10W ±5%	PHILIPS	9C0603–J000
6		18 Ω	R16,R17,R19,R22,R26,R31	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A180–JK
5		50 Ω	R12,R14,R20,R30,R32	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A500–JK
1		68 Ω	R11	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A680–JK
1		75 Ω	R33	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A750–JK
3		100 Ω	R1,R2,R6	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A101–JK
1		560 Ω	R9	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A561–JK
1		7.5 kΩ	R18	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A752–JK
1		9.1 kΩ	R27	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A912–JK
1		10 kΩ	R36	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A103–JK
2		12 kΩ	R4,R8	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A123–JK
1		18 kΩ	R25	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A183–JK
1		33 kΩ	R37	RES CHIP 0603 1/10W ±5%	PHILIPS	9C08052A333–JK
2		OPEN	R7,R28			
				Surface Mount Resistor Trimmer		
1		5 k	VR1	3mm 1 Turn J–H Trimmer	TOCOS	G3A502M
1		20 k	VR2	3mm 1 Turn J–H Trimmer	TOCOS	G3A203M
				Surface Mount Temperature Control Crystal Oscillator		
1	5V	13 MHz	VC–TCXO	Temp. Control Crystal Oscillator	KSS	VCT201C1–13MHz.
				Surface Mount Voltage Control Oscillator		
1	3V	480 MHz	Aux. VCO	Voltage Control Oscillator	MURATA	MQE962–480
1	3V	2100 MHz	Main VCO	Voltage Control Oscillator	MURATA	MQE920–2100
				Surface Mount LED		
1		LED	D1	Surface Mount LED	LUMEX	BR1111C–TR
1		BAS16	D2	Surface Mount Diode	PHILIPS	9334 606 20185 (12NC)
				Surface Mount Integrated Circuit		
1	5V	SA8027DH	U1	2.5GHz Fractional–N–Synthe.	PHILIPS	SA8027DH
1	25V	TK11900	U2	Adjustable Voltage Regulator	TOKO	TK11900
				Miscellaneous		
1				Printed Circuit Board	PHILIPS	SA80xxDH_ Rev.2
3		SMA	Main–Out,Ref–In,Aux–Out	SMA Straight Receptacle	CONNEX	132134
1		Header		Single Row Header 36 Pins	WALDOM	538–22–03–2121

Figure 31. Bill of materials.

10.0 Printer port interface schematic

Figure 32 shows the schematic of the interface card that is used to connect the evaluation board with the PC via the printer port.

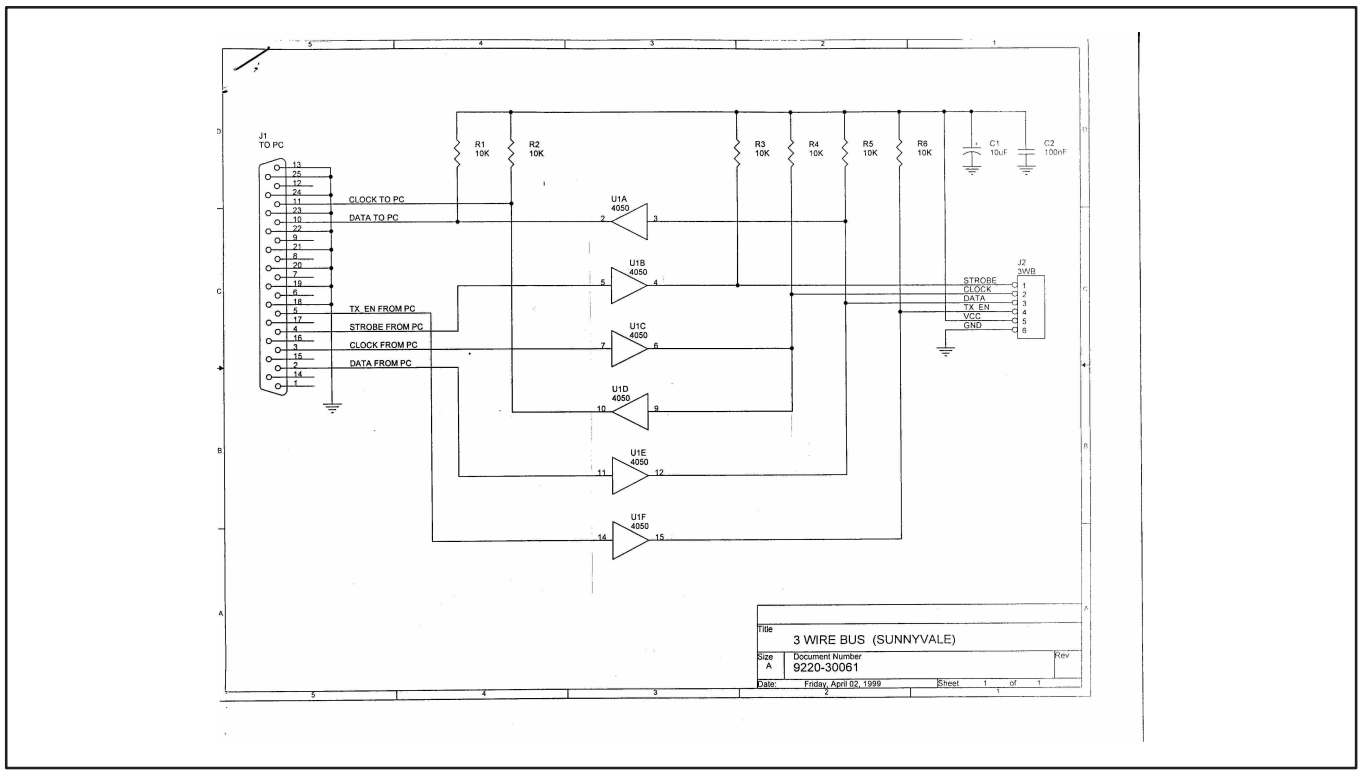


Figure 32. Interface card schematic

11.0 Questions & Answers

Q: What would cause the device to latch up and not program?

A: The device may have inadvertently entered the test mode which will make the device appear to be unresponsive. This may lead to the incorrect conclusion that the part is not working. If this were to occur, the SA8027 can be restored to normal mode of operation by clearing the D word, i.e. by programming “all–zeroes” into this register. When working with the SA8027 on the bench, simply connecting or disconnecting the control cable from the evaluation board could result in spurious programming of the D word.

Q: What should be done with unused IC pins?

A: Unused inputs, such as Rfin+ and Rfin–, should be AC grounded. The test pin should be connected to either ground or V_{DD}. Unused outputs, such as PHI and PHA should be disabled via software and floated.

Q: Will fractional compensation vary from device to device?

A: Yes, however optimum compensation can be obtained by calibrating the FDAC value over frequency and temperature during the manufacturing process.

Q: I measured the VCO phase noise at 100 kHz at –110 dBc. My VCO spec is –119 dBc/Hz. Why am I measuring –110 dBc/Hz?

A:. Noise floor limitation of the measurement equipment, the supply to VCO has insufficient filtering, and the noise contribution of the loop filter resistors can all contribute to the degradation of the VCO phase noise performance outside the loop bandwidth.

Q: After calculating loop filter values, it was found that there is little to no improvement in speed up. What went wrong?

A: The wrong charge pump gain was used or the strobe width hasn’t been widened enough to make a difference.

Q: What can cause the main comparison spur to be at a high level.

A: Large comparison spurs may be related to board layout and/or the dielectric of capacitors. The loop filter could be leaky. There may be a need to use a third order loop filter to reduce the spur amplitude further.

Q: The synthesizer will deliver a compliance voltage of only 3 volts. I have a VCO needing 5 volts compliance. What will I need to raise this potential above the 3 volt limitation?

A: An external active integrator that can deliver up to 5 volts is required.

Q: After calculating the loop filter for 200 uS why am I finding the switching time longer than expected?

A: Since the switching time is in the low micro second range it will not take much stray capacitance to influence the switching time due to the small capacitor values needed in the loop filter. One source that may go unsuspected is the VCO control pin. This VCO input pin could have a capacitance as high as 30 pF. This is enough to offset the expected time that the loop should settle.

Q: I see spurs that are neither fractional nor comparison spurs. What are they?

A: Since the VCO control line is normally in a high impedance state it can be influenced by noise sources on and near the bench. Common sources of noise can be related to:

1. Computer monitor. The scan rate of the monitor, which can range from 30 to 40 kHz, can be either radiated or conducted through the control cable from the interface board to the evaluation board.
2. Free running Auxiliary VCO. If the auxiliary VCO is enabled and out of lock, then this will show up as a noise modulation on the main VCO.
3. Fluorescent lamps. Fluorescent lamps are a good source of wide band noise.

SA8027: 2.5 GHz RF fractional-N 550 MHz IF integer frequency synthesizer

AN10159

Q: How can the residual FM noise be improved?

A: Residual FM can be reduced by using a narrower loop filter or using a higher reference frequency. The use of a higher reference frequency will reduce the charge pump ON time therefore reducing noise introduced by the pump.

Q: I am using a reference of 25 MHz and I want to use a count of 21 in the reference divider. This gives an f_{comp} of 1.19 MHz. I need 150 MHz on the auxiliary VCO, but this gives an auxiliary divide ratio of 126. Since the minimum divide ratio is 128 how can I set up the device to have a larger divide ratio and still use the 150 MHz design frequency?

A: Use the “SA” register. Set this register, located in the C word, to “1”. This will divide the f_{comp} frequency by 2, delivering 595 kHz to the auxiliary phase detector and forcing a larger divider ratio in the auxiliary divider. This brings the divider to 252 which is well within the range of the divider.

Contact information

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Date of release: 08-02

Document order number: 9397 750 10237

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